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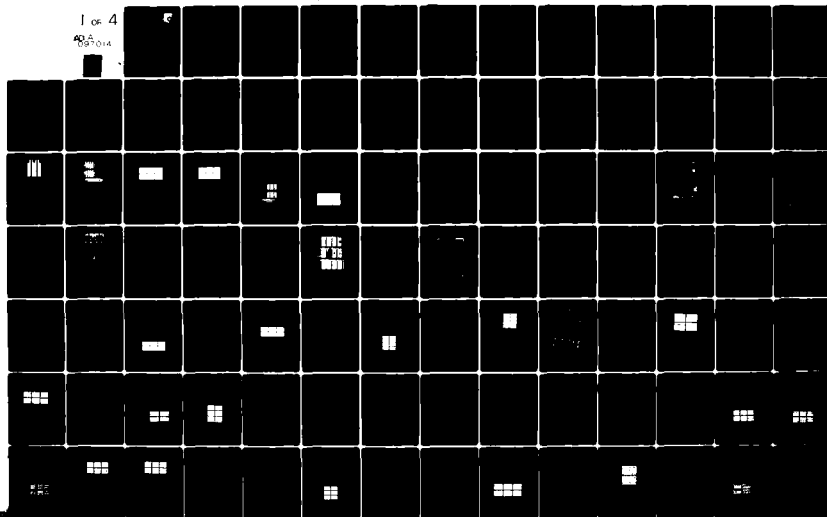
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Mayo Clinic/Mayo Foundation  
Special Purpose Processor Development Group  
Biodynamics Research Unit  
Rochester, Minnesota 55901

NOVEMBER 1980

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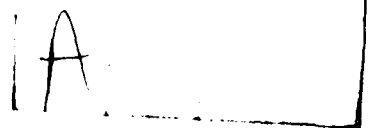
## FOREWORD

This interim report summarizes work performed under the first year of Contract F33615-79-C-1875 from the Air Force Avionics Laboratory to develop fabrication and design protocols, appropriate components and materials, as well as computer aided design software, to allow rapid fabrication of prototype special purpose processors based upon high speed subnanosecond emitter coupled logic (ECL). This work has been performed by members of the Special Purpose Processor Development Group, Biodynamics Research Unit, Mayo Clinic/Mayo Foundation, Rochester, Minnesota, and has been administered by the Air Force Avionics Laboratory, Wright Patterson Air Force Base, Ohio, Mr. William A. Anderson (AFAL/AADE-3), Contract Monitor.

The report was submitted by the authors on December 1, 1980, and covers the interim report period from July 1, 1979, through June 30, 1980. The work was performed under the principal investigator, Barry K. Gilbert, Ph.D., Director of the Special Purpose Processor Development Group, Mayo Clinic/Mayo Foundation. The following members of the Special Purpose Processor Development Group have both participated in the performance of the work under this project and have also assisted in the preparation of the text and figures in the body of this report:

L. M. Krueger: ECL Design Protocols and Special Components  
T. M. Kinter: Computer Aided Design Software  
W. F. Sutterer: Fiber Optics Transmission Techniques  
R. D. Beistad: Engineering Demonstration Test Circuit Design  
A. Chu: Algorithms and CAD Optimization Routines  
D. J. Schwab: Fabrication and Checkout of Demonstration Circuits

Subsequent interim reports under this contract will discuss conversion to encapsulation of ECL due to leadless chip carrier packaging, and to expansions of the computer aided design software in support of large configurable gate arrays fabricated with the emitter coupled logic device technology.



## ABSTRACT

This report describes the results of work conducted in the first year of a four year program to develop rapid methods for designing and prototyping high speed digital processor systems using subnanosecond emitter coupled logic (ECL). The first year effort has been divided into two separate tasks. In Task 1, described in Part I of this report, we attempted to develop a comprehensive set of design rules, interconnection protocols, special components, and standard logic panels which would allow digital processors operating reliably at clock rates in excess of 100 MHz to be quickly and easily fabricated in a one-of-a-kind, system prototype environment. We also attempted to assess the maximum operating limits of this technology, and to propose possible approaches to increasing these operational maxima. Task 2, described in Part II of this report, was to develop a comprehensive computer-aided design/computer aided manufacturing (CAD/CAM) software package which would be specifically tailored to support the peculiar design requirements of processors operating in a high clock rate, transmission line environment. The CAD/CAM software package has been structured to be sufficiently flexible to assimilate advances in device and component technology and to accept new sets of design rules resulting from advances in engineering design practice. It is our intention that this CAD/CAM capability will continue to grow in sophistication during the next three years of the project, gradually incorporating operator-interactive design aids which will allow hierarchical block-level design extending down to the integrated circuit level.

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## ECL TECHNOLOGY STUDIES

### SECTION 1

#### Introduction

During the last five years both the biomedical and military image and signal processing communities have recognized the need for very powerful, yet compact, special purpose digital computers to execute arithmetic-intensive image and signal processing algorithms. In many cases the computation rates of these special purpose processors can be augmented by exploiting inherent numerical parallelism in the algorithm, in which the complete processor is configured as a group of sub-processors, each executing a portion of the entire process. In the best cases, throughput is enhanced by a factor equal to the parallelism of the processor design.

#### Requirements for Fast Components in Large-Demand Computational Environments

An advantage of parallel processing computer architectures is the ability to increase throughput by augmentation of the processor with additional hardware subunits, a procedure that, in principle, can be extended until the number of processor subunits is equal to the maximum number of simultaneously executable subtasks. In practice, the benefits accrued from such



an augmentation diminish rapidly as shared data buses within these architectures approach saturation, and particularly, as control functions become more widely distributed and hence more complex. Further, in the initial development phase of any new or prototype computer, the advantages of installing additional subunits into such a processor are inversely related to the component count of each subunit and thereby directly related to the level of integration of the circuit technology employed. This relationship appears to hold true because the number of engineering design and fabrication errors which must ultimately be identified and corrected increases directly, both with the number of individual components in a system and with the number of discrete interconnections between these components, but not with the average integration level of the integrated circuits. In extreme cases the very complexity of a large interconnect matrix can cause some degradation in system throughput and noise margins. Alternately, or in support of improvements achieved by increasing overall machine parallelism, enhancements in processor throughput can be achieved by application of a component technology with shorter average propagation delays and/or higher integration levels.

#### Performance Comparisons and Design Constraints of TTL and ECL

Modern families of emitter coupled logic (ECL) demonstrate considerable speed advantages over the more familiar transistor-

transistor logic (TTL), both on a gate-by-gate basis for logic and arithmetic elements and in decreased cycle times for static random access memory as well. The most commonly used ECL family, ECL 10K, introduced in the early 1970's, displays gate propagation delays and risetimes of 2 ns and device speeds three to four times greater than conventional TTL for equivalent levels of integration. Recently, several advanced families of ECL have been introduced which exhibit subnanosecond gate propagation delays and risetimes; these devices promise nearly an order of magnitude improvement in throughput over conventional TTL technology and can be integrated to very large scale integrated (VLSI) circuit density levels. Four vendors are currently producing subnanosecond ECL components. A complete set of SSI and MSI devices, and an increasing number of LSI devices, are available from Fairchild Camera and Instrument Corporation; Signetics-RTC Inc. (a subsidiary of Phillips Corporation) is aggressively initiating a second source effort. Siemens, Inc. offers a small but complementary line of LSI devices, and is also initiating second source agreements with Fairchild. Hitachi, Ltd., a Japanese vendor, manufactures subnanosecond ECL devices of its own design.

The potential of these new subnanosecond ECL technologies is somewhat diminished by the special measures thought to be necessary to interconnect components exhibiting subnanosecond wavefronts and gate propagation delays. Expensive multilayer circuit boards (containing as many as 15-20 signal, power, and

ground layers) with controlled impedance signal lines (fabricated with stripline and microstrip techniques) have been exploited to minimize wavefront reflections and overshoot, in combination with sophisticated computer-aided design (CAD) methods which simulate operation of selected subsystems on a wavefront basis. However, the frequent requirement to make numerous engineering changes during the development of prototype high performance signal processing systems will restrict the use of subnanosecond ECL for new designs unless viable but simplified fabrication techniques can be identified which preserve the high performance of the logic.

## PART I

### DEVELOPMENT OF INTERCONNECT PROTOCOLS AND COMPONENTS SUITABLE FOR USE WITH SUBNANOSECOND ECL IN A SYSTEM PROTOTYPE ENVIRONMENT

Because the fabrication of recently developed high speed signal processing and image processing architectures using subnanosecond ECL would result in a performance improvement in many of these processors by a factor of at least four, we have investigated several packaging and system fabrication techniques for subnanosecond components which circumvent the requirement for multilayer printed circuit boards for use in prototype processor designs, while maintaining the capacity for operation at very high clock rates. The fabrication technique is a refined version of the "wire wrap" interconnect method developed in the early 1960's for TTL and later modified by us (Reference 1) and others in the early 1970's to accomodate the 2 nsec ECL introduced in 1971 by Motorola, Incorporated. The laboratory studies, component development projects, and specialized computer-aided design (CAD) software packages described in this report have resulted in a set of specific guidelines for the fabrication of large one-of-a-kind high performance prototype processors using subnanosecond ECL components, with all interconnects via this modified wire wrap interconnect technology. Early in the development cycle it became evident that these protocols would be too complex to allow manual layout of

systems in which all interconnects must be treated as transmission lines, requiring attention to the problems created by signal stubs, destination drops, signal loading, and appropriate termination. Attempts to create such layouts manually demonstrated clearly that computer-aided design software packages optimized for these protocols would be required to achieve proper layout and subsequent fabrication of processors exploiting high speed ECL.

#### Examination of the "Stitch-Weld" Fabrication Technique

We investigated the possibility of employing the open wire interconnect technique referred to as "stitch weld". Although one paper in the technical literature does describe the interconnect of subnanosecond ECL components using stitch weld (Reference 2), our conversations with several of the groups using this interconnect approach revealed several serious deficiencies. First, as will be demonstrated later, the use of twisted pair wires to improve the transmission line characteristics of the interconnects in turn improves the performance of ECL-based systems considerably, in comparison with single wire interconnects. It is extremely difficult (though not totally infeasible) to employ twisted pair wiring protocols with the stitch weld technique. In addition, removal of a wired string already in place on a stitch weld circuit board is cumbersome, since the entire string must be removed from the weld point contacts with a special shearing tool, and then

replaced with a completely new set of wires. The replacement task frequently damages other wired structures on the board, resulting in an inability to make rapid modifications on a single circuit board while maintaining high transmission line uniformity. Since we were able to demonstrate that a modified wire wrap technology works extremely well in this high speed device environment, the stitch weld interconnect approach was not pursued.

## SECTION 2

### Initial Feasibility Studies of Wire Wrap Interconnect Techniques

Initial investigations of the feasibility of wire wrap fabrication techniques for subnanosecond ECL were based upon measurements recorded from a small subnanosecond ECL circuit designed in several experimental versions using early engineering prototype 24-pin dual in-line ceramic packages. This circuit, assembled from components donated by the original vendor, Fairchild Camera and Instrument Corporation, consisted of a five stage ring oscillator operating at clock rates which varied from approximately 40 MHz to 280 MHz, which in turn was used to clock a 12-bit binary counter. The frequency of the ring oscillator was tuned by changing the length of interconnect wire between two of the gates in the ring oscillator. The data bits from the counter, which was clocked by the ring oscillator, were in turn stored in a group of D-type registers. Figure 1 is a photograph of the first of these prototype circuits, fabricated on a small two layer wire wrap card. Note the two rows of integrated circuits, and the placement of decoupling capacitors between the ground plane and the -4.5 volt  $V_{EE}$  plane, and the -2 volt  $V_{TT}$  plane. Figure 2 shows the wire wrap side of this same circuit board. To create power planes for both the -2 volt and -4.5 volt buses, the plane on the component side of the card was committed to the -2 V supply, and a heavy strip of copper sheet was cut and then positioned several millimeters

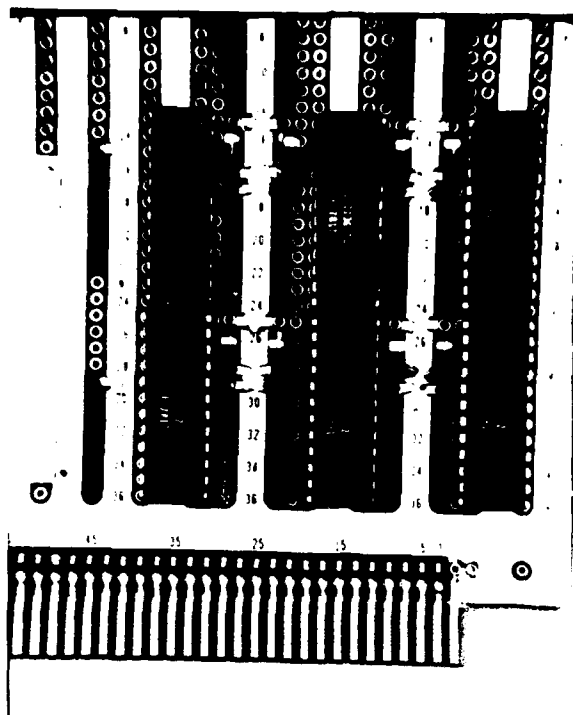


Figure 1  
FIRST PROTOTYPE SUBNANOSECOND ECL  
CIRCUIT FABRICATED WITH WIRE WRAP

above the surface of the board to serve as the  $-4.5$  V bus. No attempt was made in this first prototype to achieve uniformity of the ground and power plane layouts, or to insure short return paths for the signals. Figure 3 shows measurements from this initial circuit with a clock rate generated by the ring oscillator of 37 MHz. In the lower leftmost panel, the 20-80% rise-time is approximately 800 psec, and the clock waveform appears to be relatively free of contaminating noise; however, ringing is apparent following the rising and falling edges of the



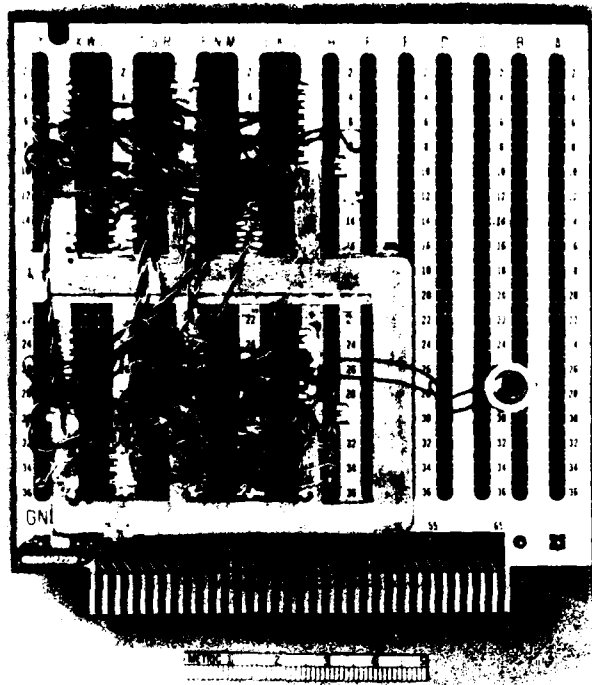
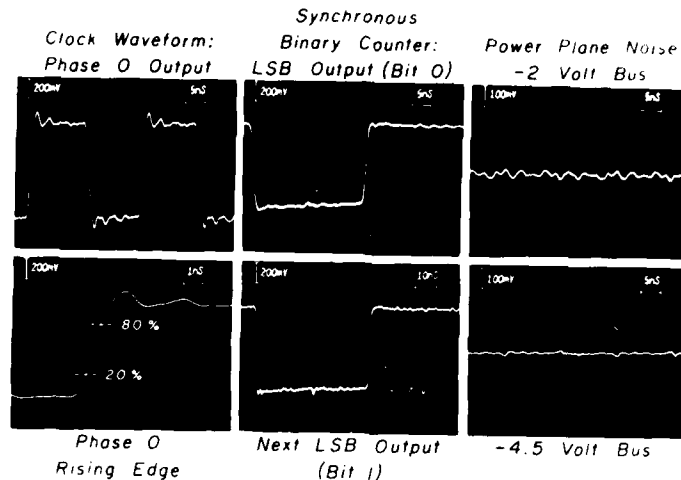


Figure 2  
WIRE WRAP SIDE OF PROTOTYPE ECL  
CIRCUIT SHOWING HEAVY COPPER -4.5 V BUS

waveform. The two least significant bit outputs from the synchronous binary counter also were relatively free of noise. The -2 V and -4.5 V power plane noise was considerably less than 100 mV peak-to-peak.

When the clock rate of the ring oscillator was increased to frequencies between 180 MHz and 280 MHz, the results were considerably different. Figure 4, depicting measurements from the same test circuit but operated at a clock rate of 180 MHz, demonstrates several problems which had to be circumvented

OPERATION OF PROTOTYPE SYNCHRONOUS  
DIGITAL CIRCUIT FABRICATED WITH  
SUBNANOSECOND EMITTER COUPLED LOGIC (ECL)  
(37 MHz System Clock Generated via Ring Oscillator)

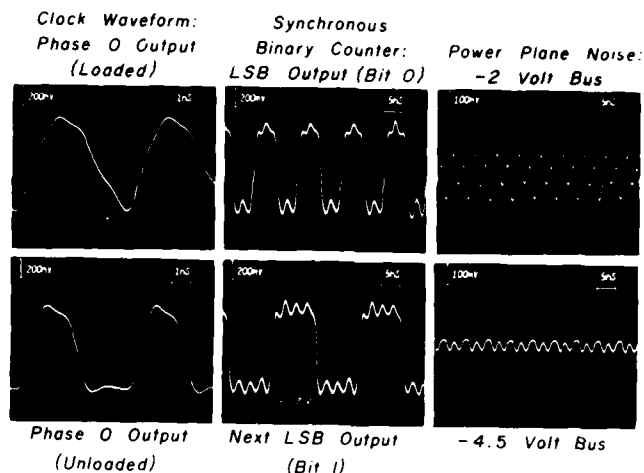


\* Outputs Terminated, via 82 Ohm Resistor Networks

Figure 3

before large scale systems could be fabricated with a wire wrap technology. Note the subnanosecond rise and fall times in the lower left panel and the low level of overshoot (less than 15%) on the waveform edges. However, considerable differences in waveshape are observed at the outputs of loaded and unloaded driving gates representing the same clock phase (upper and lower leftmost panels). The middle panels of this figure demonstrate that the counter correctly followed the 180 MHz clock input, although the waveforms demonstrate a considerable amount of "noise" or "crosstalk" which degrades system noise margins. In the lower right panel of Figure 4, the

OPERATION OF PROTOTYPE SYNCHRONOUS  
DIGITAL CIRCUIT FABRICATED WITH  
SUBNANOSECOND EMITTER COUPLED LOGIC (ECL)  
(180 MHz System Clock Generated via Ring Oscillator)



All Outputs Terminated, via 82 Ohm Resistor Networks

Figure 4

-4.5 V power bus exhibits a peak-to-peak noise of approximately 50 mV, an "acceptable" level since the integrated circuits themselves contain internal voltage compensation networks for the -4.5 V bus, and in addition use a complementary transistor design which minimizes fluctuations in the instantaneous current requirements from this bus. However, in the upper right panel of Figure 4, the noise on the -2 V bus is considerably larger in amplitude (>100 mV peak-to-peak) and of greater consequence since the -2 V bus serves as the reference voltage plane for the logic LOW level (Reference 3). The effects of local voltage fluctuations on the -2 V bus can be observed on

the upper and lower portions of the signals in the middle panels of Figure 4. An additional source of contamination was introduced by the termination networks themselves if standard commercially available terminator packs rather than discrete or buried layer resistors were employed. A further explanation of and solution for the problem of noise "generated" by the terminator networks will be described below.

Based upon these measurements, it appeared that inadequate ground and power plane continuity and insufficient decoupling of the ECL integrated circuits at every component location were

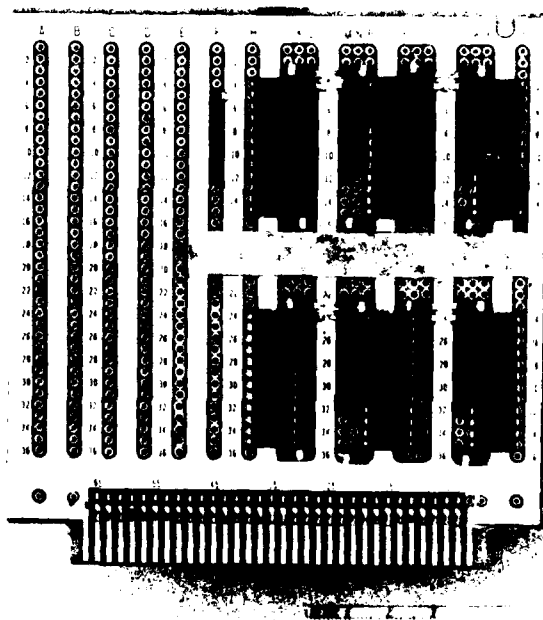
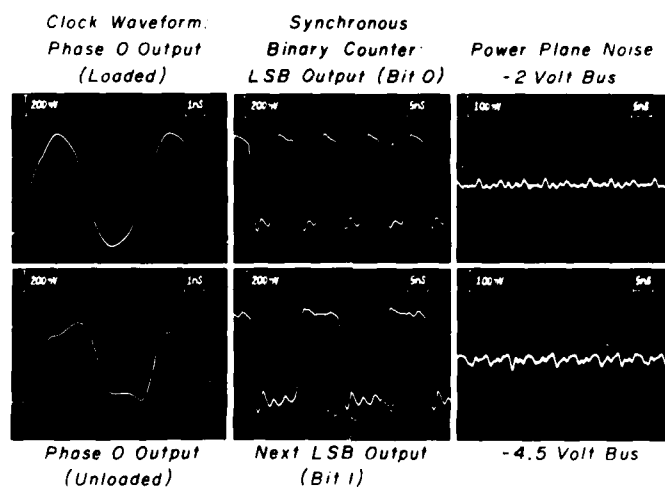


Figure 5  
SECOND PROTOTYPE SUBNANOSECOND ECL  
CIRCUIT FABRICATED WITH WIRE WRAP

responsible for the significant amount of noise observed on the -2 V bus in Figure 4. Accordingly, the small test circuit was rebuilt, to the configuration depicted in Figure 5. The two rows of integrated circuits were separated by a wide, horizontally running band of metal foil; decoupling of the power planes at each integrated circuit location was also improved. Figure 6 depicts results from the same circuit operating at 185 MHz, with measurements at the same test point locations used for Figure 4. Note that the loaded phase 0 clock waveform in the upper leftmost panel is somewhat less triangular, and the peak-to-peak noise on the logic HIGH and LOW portions

OPERATION OF PROTOTYPE SYNCHRONOUS  
DIGITAL CIRCUIT FABRICATED WITH  
SUBNANOSECOND EMITTER COUPLED LOGIC (ECL)  
(185 MHz System Clock Generated via Ring Oscillator)



All outputs terminated via 100 Ohm Resistor Networks

Figure 6

of the waveforms in the center panels is of lower amplitude, particularly in the logic HIGH state. More significantly, the power plane noise on the -2 V bus has decreased from 200 mV to approximately 50 mV peak-to-peak. This improvement in power plane noise indicates the importance of a high degree of continuity throughout the ground and power planes, a finding which was reconfirmed in other test circuit configurations described later.

Why Does Subnanosecond ECL System Design Require More Care Than 2 Nsec ECL System Design?

The experiments described in the preceeding paragraphs have demonstrated unequivocally that processor systems fabricated with subnanosecond ECL require considerably more stringent design and layout rules than those for conventional TTL logic, or even for earlier families of ECL exhibiting 2 nsec risetimes; if subnanosecond ECL systems are fabricated with wiring rules for 2 nsec ECL, overall operation is noisy and unstable, as depicted in Figures 4 and 6. It is reasonable to question why more care must be exercised in the use of subnanosecond ECL, and how much more serious these problems are likely to be. Short of a comprehensive analysis of these problems, it is nonetheless possible to estimate the impact of the operational characteristics of subnanosecond ECL on interwire crosstalk, degradation of signal wavefronts by reflections, and so on.

Interwire crosstalk is caused by electromagnetic coupling between two signal strings positioned parallel to one another. An examination of the laws of Ampere, Biot-Savart, Lenz, and Faraday demonstrates that a crosstalk voltage  $E$  electromagnetically induced between one current-carrying interconnect and a second interconnect is proportional to the time rate of change of total flux  $\frac{d\phi}{dt}$  generated by the first wire which intersects the second. The magnitude of the intersecting flux is in turn related to the rate of change of current flowing through the first wire. In a subnanosecond ECL signal string, the typical characteristic line impedance is maintained at as low a value as possible (see Part I, Section 3), usually 50 to 75 ohms, compared to a nominal line impedance of 100 ohms commonly used in 2 nsec ECL. However, the logic level swing is approximately 20% less for subnanosecond ECL than for 2 nsec ECL. Hence, the average amount of current switched during a logic transition of a subnanosecond ECL logic string is approximately 1.07-1.6 times larger than for an equivalent 2 nsec ECL logic string. Further, the risetime of the subnanosecond ECL signal is only 25% that of the 2 nsec ECL gate; as a result of these differences in risetimes, 1.07 to 1.6 times as much current is switched within a duration of 500 psec rather than 2 nsec. In turn,  $\frac{d\phi}{dt}$  will be 4.25 to 6.4 times greater for the subnanosecond ECL logic string than for a 2 nsec ECL logic string, resulting in increased electromagnetic crosstalk levels of 4.25-6.4, all other factors remaining equal. Hence, to maintain a fixed level of crosstalk immunity, layout and interconnect protocols

will have to be five to seven times more stringent for subnanosecond ECL than for 2 nsec ECL.

The effects of wavefront reflections on signal integrity can be roughly estimated by recognizing that these reflections will have little effect if the round trip propagation delay throughout the length of the signal string is much less than the risetime of the typical signal wavefront. Assuming for this discussion that "much less" can be assumed to be half the signal risetime, the round trip signal string delay must be restricted to 250 psec for subnanosecond ECL and 1 nsec for 2 nsec ECL. With a wire propagation delay of 125 psec/inch for open wire lines, reflections can degrade signal integrity for subnanosecond ECL signal strings longer than approximately one inch, and for 2 nsec ECL signal strings longer than four inches. Physical layout constraints of wire routing indicate that, to a crude first approximation, subnanosecond ECL signal strings will suffer from reflection-induced wavefront degradation four times more frequently (or four times more seriously) than will 2 nsec ECL signal strings.

The previous two examples, though somewhat simplistically stated, illustrate exemplary reasons why subnanosecond ECL must be used with greater care than 2 nsec ECL or TTL logic families. As a rough rule of thumb, the magnitudes of each and every source of signal contamination such as electromagnetic crosstalk appear



to be approximately five to ten times more damaging in subnanosecond ECL systems than in 2 nsec ECL systems. It is the severity of these parasitic noise effects which account for the poor results of our early studies as depicted in Figures 4 and 6, and which have motivated the careful development of design and layout protocols, special components, and logic boards described in the following sections of this report.

### SECTION 3

#### COMPONENTS AND LOGIC PANELS FOR SUBNANOSECOND ECL SYSTEMS

##### Decoupling Capacitors for Subnanosecond ECL---Type and Placement

Figure 7 depicts two types of power plane decoupling capacitors (labeled f and g in this figure) whose high frequency operating characteristics are compatible with subnanosecond ECL integrated circuits (labeled h in this figure). The component labeled f is a 100 VDC, 0.01  $\mu$ F capacitor (AVX Ceramics Corporation DG011C 103M), fabricated with Type X7R ceramic dielectric, which is employed to decouple the -4.5 V power bus. This capacitor, which was the only available design during the initial portion of this work, can now be replaced by a newer design from the same vendor (AVX Ceramics Corporation DG015C 104M) with a 50 VDC, 0.1  $\mu$ F rating. Part g, employed to decouple the -2 V bus, is a low voltage 3.3  $\mu$ F 10 VDC tantalum electrolytic capacitor of superior high frequency characteristics (Fujitsu CS90E-IA-3R300-R58). The optimum ratio of decoupling components to digital circuits and the placement of these decoupling components relative to the locations of the integrated circuits was investigated using subnanosecond ECL test circuits operating at clock rates of 250 MHz. These tests indicated that a decoupling capacitor more than a few centimeters from a subnanosecond ECL integrated circuit is nearly "invisible" to that circuit. For

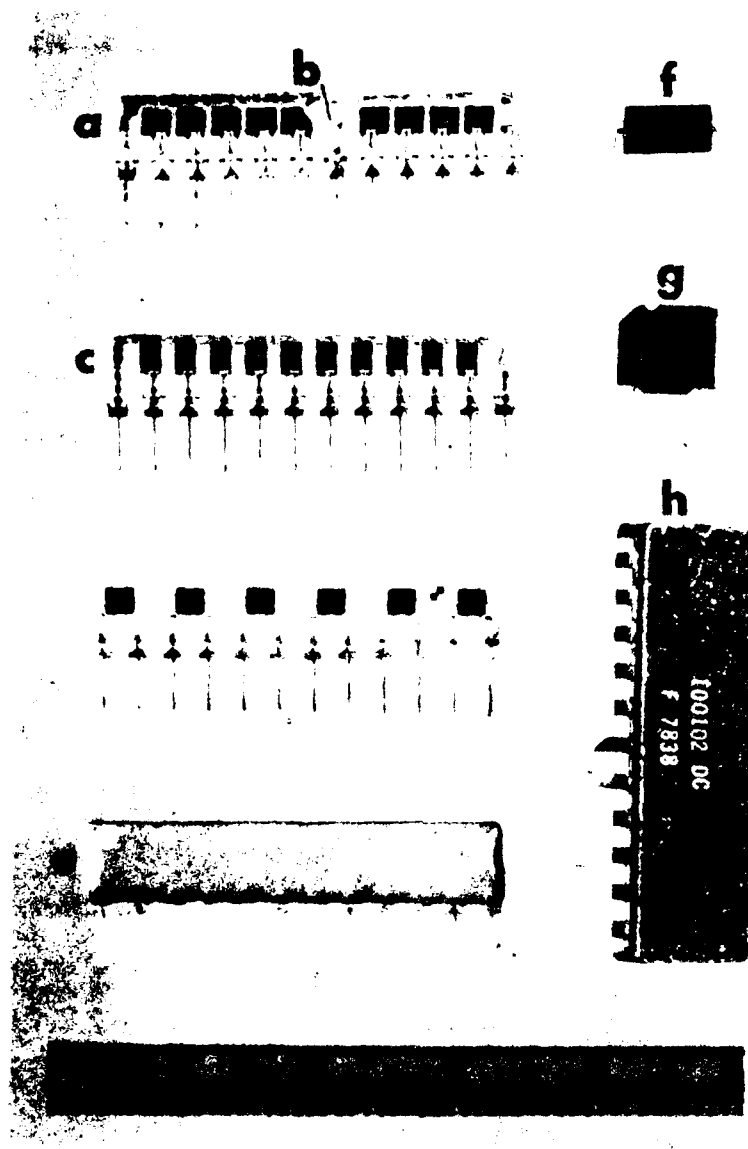


Figure 7  
 SUBNANOSECOND ECL IN 24 PIN CERDIP,  
 DECOUPLING CAPACITORS, AND  
 SPECIALLY DESIGNED TERMINATOR NETWORKS

the frequency components near 1 GHz generated by the subnanosecond risetimes of the 100K ECL components, the several nanohenrys of inductance of the power plane foil and decoupling capacitor leads are equivalent to a series impedance of several tens of ohms. The resonant frequency of the series LC circuit formed by this combination is less than 10 MHz, i.e., far less than the operating frequencies under consideration here; hence, the series inductive effects of the foil and component leads are dominant. Therefore, the effectiveness of a decoupling capacitor several centimeters from any given integrated circuit is almost nil. It is thus necessary to assure that a decoupling capacitor for each voltage bus is in close proximity to every integrated circuit.

#### Logic Panel and Ancillary Component Designs

Using time domain reflectometry and direct measurement techniques, the desirable physical and electrical characteristics for a wire wrapped logic panel and ancillary components (decoupling capacitors and terminator networks) suitable for use with subnanosecond ECL dual in-line packages were developed. Based upon these measurements, the appropriate boards and components were identified, or designed in-house if not available commercially. Fabrication of the Mayo-designed components was subcontracted to several vendors (Augat, Inc., for the boards, and Epitek, Inc., for the terminator components).

## Design of Large Wire Wrapped Logic Panel

Component side: Figure 8 depicts an unpopulated portion of the component side (the ground plane side) of a five-layer, three-plane logic panel for subnanosecond ECL components in 24-pin dual in-line packages. The 10-25 mA currents which flow in each low impedance ECL signal line are accompanied by equivalent "return-path" currents flowing in the power and ground planes. A sufficient number of low impedance A.C.

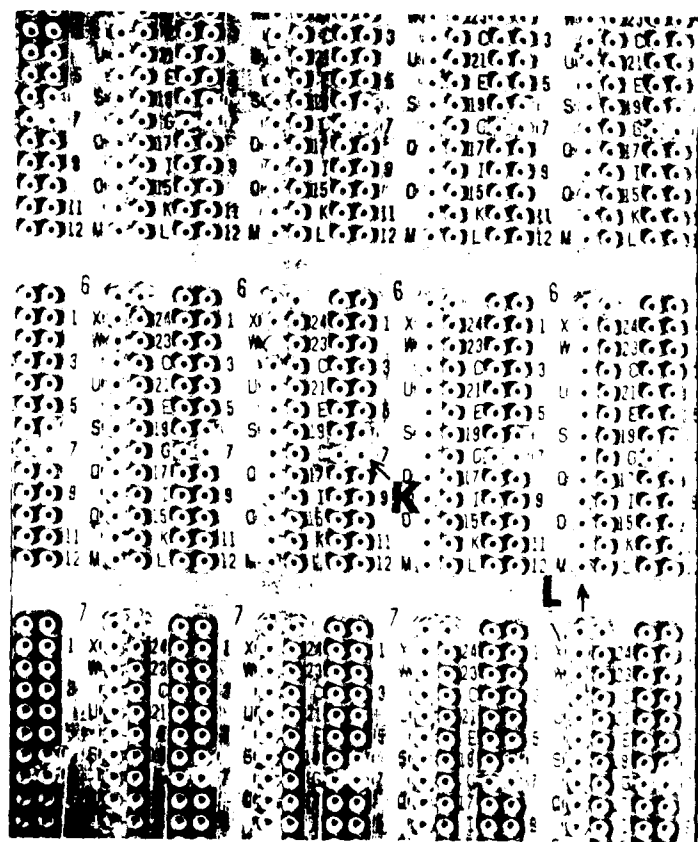


Figure 8

UNPOPULATED COMPONENT SIDE OF MAYO-DESIGNED  
LOGIC PANEL FOR 100K ECL DEVICES PACKAGED IN 24-PIN DIP

ground return paths must be provided within the power and ground plane foils to suppress short duration local variations in the power plane voltages, which can otherwise exceed 700 mV peak-to-peak over 2-4 cm separations on any given plane.

The operational tests described in Section 2 demonstrated the necessity for wide horizontally and vertically running foil paths passing beneath and between the integrated circuits. Although the extra area allotted for foil increases board dimensions in both the X and Y dimensions by 5-10%, the additional foil significantly decreases series impedances in the power and ground plane return paths. Because of the flared shape of the socket pin heads, it is not feasible to pass ground foil between the pin heads in a horizontal or vertical direction if a center-to-center pin spacing of 0.1 inch is employed. To minimize the length of return paths on the component side, note that at letter K in Figure 8 the ground foil is continued horizontally across the integrated circuit pins 6 and 7 and terminator pin 7. The wire wrap pins in the column labeled L are committed to ground during fabrication of the logic panel to serve as the attachment points for ground wires in the twisted pair interconnects.

Logic Panel Buried-Layer Plane and Backplane: Figure 9 depicts the unwired backplane of the large Mayo-designed three-plane logic panel designed for subnanosecond ECL circuits (Augat, Inc. Part #X8136-ECL-117-2). A concerted effort was made to provide

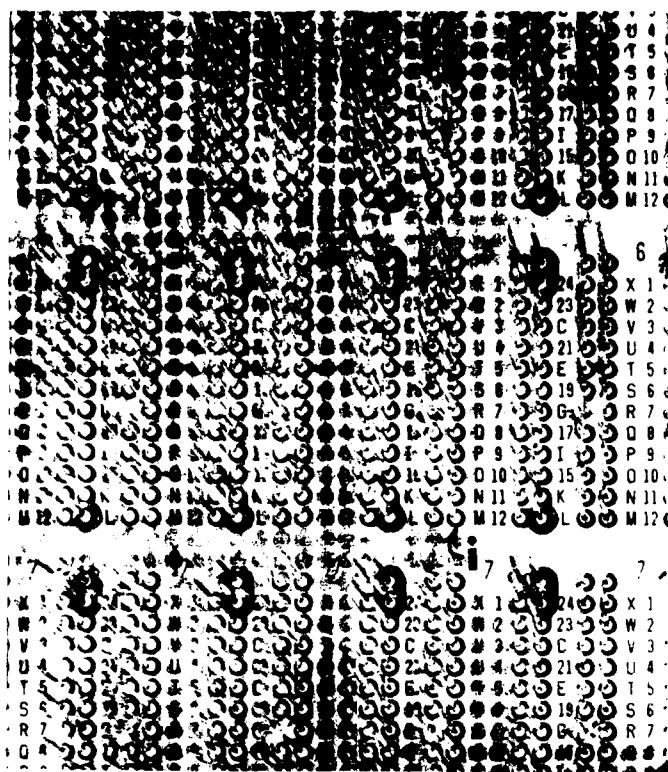


Figure 9

WIRE WRAP SIDE OF MAYO-DESIGNED ECL LOGIC PANEL  
SHOWING EXTENSIVE FOIL CONTINUITY OVER ENTIRE BACKPLANE

a maximum amount of foil for return path currents throughout the logic panel. To maximize the integrity of both the wire wrap side foil (the -4.5 V plane) and the buried-layer foil (the -2 V plane), at letter i the socket pins protrude through circular "holes" etched through the 3 oz copper foil. The use of two-level wire wrap pins rather than three-level pins discourages the addition during engineering modifications of a third wire to a pin, thus creating an unterminated transmission line stub or an overterminated Y-configured signal string.

## Design of Terminator Packages

Two completely different approaches appeared viable for the design of terminators to be used with this high speed logic family. First, a specialized layer of the multilayer wire wrap board could have been dedicated to these terminator resistors. Second, pack terminators could be designed and merely plugged or soldered into the board at the required locations. A terminator plane layer is generally employed in multilayer printed circuit board environments because circuit board real estate need not be allocated to the terminators themselves. However, it soon became apparent that in a system prototyping environment, an electrically optimum interconnect design would require the use of several different termination protocols, depending upon the type of signal being propagated, with each protocol requiring an unique interconnect topology and terminator resistance values. For a universal board design intended for prototyping applications, the possible inclusion of two or three terminator layers buried in the circuit board appeared cost-prohibitive, with no convenient way to commit the appropriate terminators to the appropriate pins in any event. Hence, we opted for the use of terminator pack resistor units of several different styles which can be plugged into the logic panels as required.

Figures 1 and 5 show the placement of several terminator packages of readily available commercial design. These terminator packages were found to have several severe limitations



because they were not designed to operate in circuits clocked at rates above 100 MHz. As a result, it was necessary for the Mayo group to design terminator packages specifically to operate at these high frequencies. The components labeled a, c, and d in Figure 7 are three separate styles of these Mayo-designed terminators intended for use in subnanosecond ECL systems, shown without their protective ceramic encapsulation. Component d (Epitek Special Part #L1206-101G) contains six individual 100 ohm resistors employed for line-to-line termination at the receiving end of a differential transmission pair. Component c (Epitek Special Part #L1211 471G) contains ten 470 ohm resistors employed to provide a "pull-down" voltage for each transmitter output for a differential pair (Reference 3). Component a (Epitek Special Part #3B14000) contains a group of nine 85 ohm terminator resistors, with one end of each resistor connected to a common internal -2 V bus, which is in turn connected to pins 1 and 12 at either end of the terminator package. A 3900 pF high frequency miniature chip capacitor (labeled b in Figure 7) is included in the Mayo-designed terminators, serving as a physical bridge between the terminator internal bus and pin 7, which is committed to the logic panel ground plane. Noise studies, to be described later in conjunction with Figure 26, demonstrated that inclusion of this small chip capacitor significantly improves the performance of the terminator network. The component labeled e in Figure 7 shows the appearance of the resistor networks with ceramic encapsulation in place. A more detailed description

of the mechanical and electrical characteristics of these specially designed terminator packs will be presented in a later section of this report entitled: "Noise Induced in Operating Signal Strings Through Pack Terminators".

Description of Populated Logic Panel: Figure 10 depicts a small section of the component side of the subnanosecond ECL circuit board with components installed. Decoupling capacitors, integrated circuits, and terminators are labeled as in Figure 7. The small carrier (Augat Part #101 HG1) observed in the center of the photograph contains two SMA miniature high frequency coax connectors, used to inject high frequency clock signals into the geometric center of each logic panel. The cable leading to the SMA connector header is miniature coax of the RG 174/179 series (described in detail later). The three-plane logic board (Augat Special Part #X8136-ECL-117-2), measuring 14.5 X 21.25 inches, contains 198 patterns in an 18-column by 11-row arrangement, as well as forty 40-pin cable connectors. Figure 11 depicts the entire logic panel, viewed from the component side, in which the 40-pin cable connectors and the 198 circuit patterns can be observed. At the right edge of the panel, multiple nut and bolt connections may be observed for the ground, -2 V, and -4.5 volt power planes. To the right of the 40-pin cable connectors, a single nut and bolt assembly allows for attachment of a +5 V power supply, if required for TTL/ECL translator components. The arrangement of socket pins in the individual integrated circuit patterns



FIGURE 10  
POPULATED SECTION OF MAYO-DESIGNED 10-MHz PANEL  
FOR ECL DEVICES IN 24-PIN FORMAT.

allows the use of either 300 mil center components or 400 mil center components in any location, now limited to the location of subnanosecond ECL logic components, and is designed for use with 24-pin ceramic dual in-line packages, which are not currently manufactured, and 24-pin center components, which are currently available in 300 mil center format.

ground-committed wire wrap pins in the column labeled L of Figure 8 can be spot-faced to decommit them from ground, and the pins in the next rightmost adjacent column can be committed to ground with special hairpin clips (Augat Part #X8136-592P2), any given socket location may be converted from a 400 mil center component to a 300 mil center component with a small amount of manual board preparation.

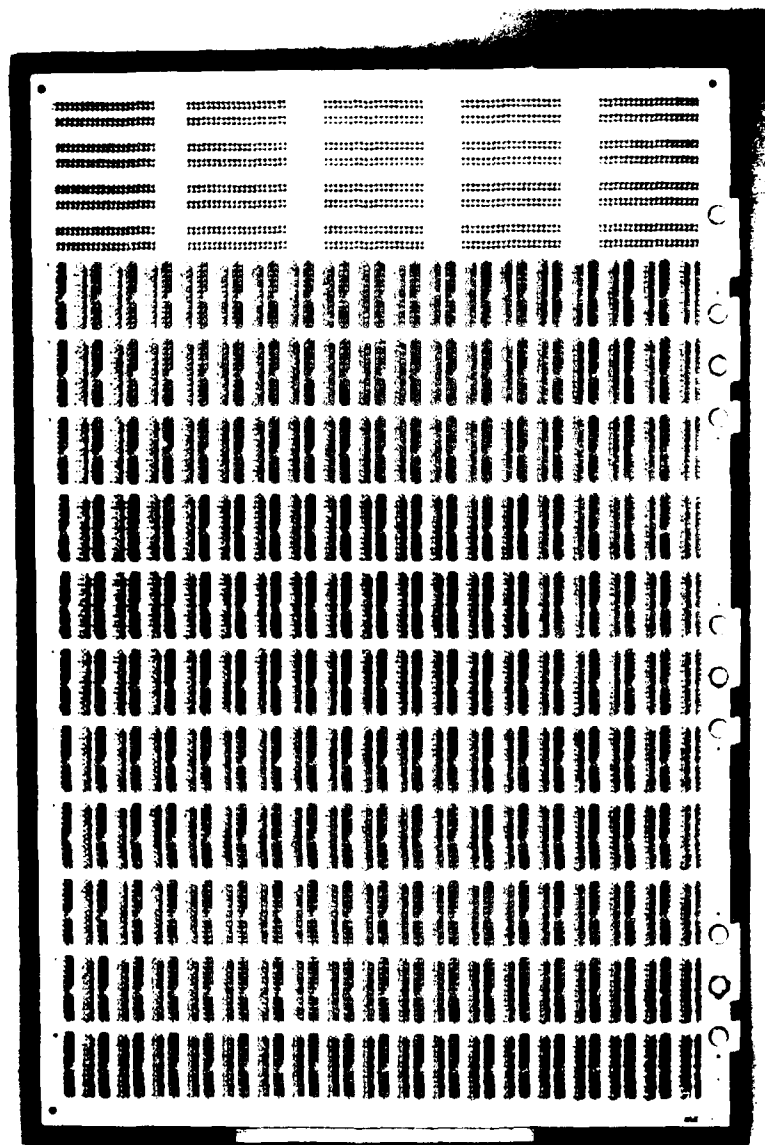


Figure 11  
 COMPONENT SIDE OF LARGE WIRE WRAPPED LOGIC PANEL  
 FOR ECL 100K COMPONENTS PACKAGED IN CERDIP

#### SECTION 4

#### STUDY OF INTRACOMPONENT AND INTRABOARD INTERCONNECT PROTOCOLS USING TIME DOMAIN REFLECTOMETRY (TDR) AND DIRECT OPERATIONAL MEASUREMENT TECHNIQUES

A variety of interconnection protocols for subnanosecond ECL components were investigated employing both direct operational measurements and time domain reflectometry techniques. For the TDR studies, a Tektronix Model 7S12/S-52/S-6 time domain reflectometer/sampler with a pulse source risetime of 35 psec was employed. All TDR measurements represent the response of the interconnect network to frequency components in the range of five to eight gigahertz, which are somewhat higher than the first few harmonics generated by the subnanosecond ECL circuits themselves. Protocols for component-to-component signal interconnects, connections between the logic panels and multiconductor cable, and mechanisms for high frequency clock signal distribution to multiple logic panels have been studied by fabricating small test circuits on the Mayo-designed logic panel depicted in Figure 11, and then performing both TDR and operational tests on these small circuits.

The fabrication of systems with low impedance short rise-time ECL devices requires that transmission line interconnects be established between individual components. In addition, local variations in transmission line impedance cause undesired

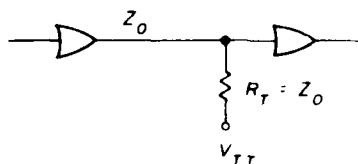
secondary wavefront reflections which degrade the edges of the intended waveforms, and in extreme cases actually cause voltage wavefront fluctuations which may cross the logic threshold and cause false triggering of components. As already described in the discussion of ECL terminations, an impedance discontinuity to a value higher than the line impedance causes a "positive" reflection voltage wavefront (i.e., with the same polarity as the primary wavefront and in a direction away from the threshold voltage), while an impedance discontinuity to a value less than the line impedance causes a "negative" reflection voltage wavefront (i.e., with a polarity opposite to the primary wavefront and toward threshold). The negative reflection is the more serious, since it directly degrades system noise margins and causes false triggering of circuits. Unfortunately, most discontinuities on an ECL transmission line are of the low impedance variety. The logic pin input to each ECL gate presents a low impedance shunt capacitance (Reference 3) across the transmission line, which is never less than 2 pF and occasionally as much as 10 pF, with equivalent shunt impedances as low as 30 ohms.

The transmission line will be least susceptible to the deleterious effects of these parasitic shunt capacitances if the line impedance is minimized, since a low impedance line will most closely match the impedances of the parasitic shunt capacitors, and hence result in a minimal impedance discontinuity and a minimal reflection (Reference 3). Stated alternately, the lower impedance lines can more quickly charge the

shunt capacitances to the value of the impinging voltage wavefront, minimizing the duration of the discontinuity. Unfortunately, low impedance line protocols (25-50 ohms) require low impedance primary termination and therefore dissipate considerable power, causing a high component operating temperature and decreased mean time to failure. Clearly, a tradeoff is required here. We attempted to achieve a balance between these conflicting constraints by using an impedance protocol as close to 75 ohms (for single ended transmission) as possible.

#### Discussion of Various Interconnect Protocols Useable in a Transmission Line Environment

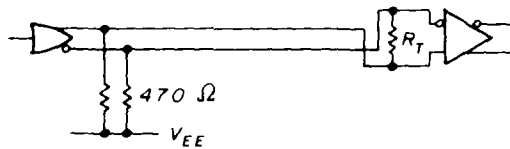
A substantial number of methods, or protocols, can be conceptualized for interconnection of nodes in a logic string if the interconnect medium must be maintained as a low impedance transmission line. Both single ended and differential approaches may be used, with party line and bus-oriented protocols also possible. A differential line pair, on which both true and complement signals are transmitted, may have only a single source and a single destination, or may have a single



SINGLE ENDED TRANSMISSION

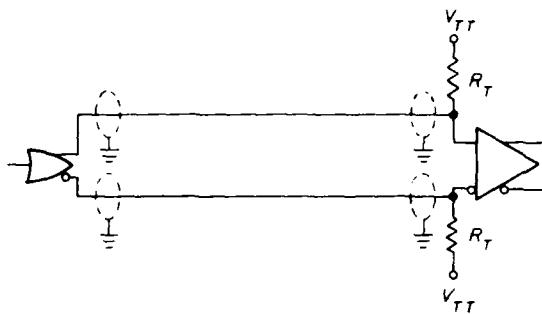


source and multiple destinations; in the latter case, if the destinations are purely sequential, the interconnect scheme



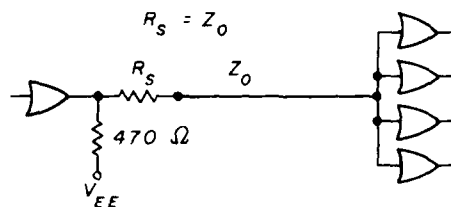
#### DIFFERENTIAL TRANSMISSION

is referred to as daisy chaining. Differential mode transmission in a low impedance ECL environment requires a terminator resistor between the true and complement sides of the line at the receiver, with a much larger resistor to a negative voltage reference, usually  $V_{EE}$ , on each leg of the differential line at the source outputs. If daisy chaining is used, the terminator is placed between the lines at the location of the final destination node. An alternate version of the differential transmission protocol, which can be used in very high noise environments (described in detail in Part I, Section 6) is differential transmission via a pair of coaxial cables, with both shields grounded at both ends. This protocol is referred to throughout the remainder of this report as "dual single-ended" transmission. Although an expensive protocol, for high value signals such as clocks, the additional stability and noise immunity of the signal transmitted in this manner may warrant the extra effort.



#### DUAL SINGLE ENDED TRANSMISSION WITH GROUNDED SHIELDS

Two types of single ended transmission protocol are feasible. A series terminated protocol places a resistor in series with the line at the output of the source gate; the line charging current actually must pass through this resistor (whose value should equal the characteristic impedance of the line) to charge the intrinsic capacitance of the transmission line and alter the line voltage. At the destination end of a series terminated line, the destination nodes are grouped as closely together as possible and are not connected to a termination resistor. Signal wavefronts are allowed to reflect from the

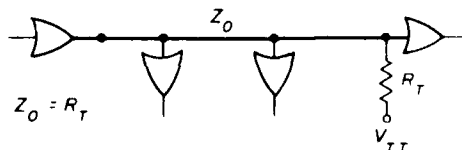


#### SERIES TERMINATION

far end of the line; all such reflections returning to the source are damped through absorption at the series source resistor. The advantage of the series termination protocol is that

multiple series-terminated lines may be fanned out in a star-wise manner from a single source gate, while the average power required to drive each line is maintained at an absolute minimum value; lastly, for ECL, only a single  $-4.5$  volt  $V_{EE}$  supply voltage is required. There are several disadvantages inherent in the series termination protocol: 1) signal risetimes are degraded by the series resistor, which prevents rapid line charging; 2) reflections from the unterminated end of the transmission line are severe (the reflections in effect double the amplitude of the incident wave, though in a direction (polarity) away from the logic threshold); 3) a slight decrease in the quiescent noise margin of the circuit in the logic HIGH state is observed, because leakage currents into the destination gate cause a slight voltage drop to appear across the series termination resistor, in turn causing the destination inputs to record a slightly lower value of the logic HIGH voltage.

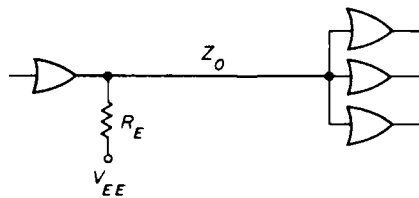
The second type of single-ended transmission protocol suitable for ECL is the parallel or shunt termination, in which the final destination node of a logic string is connected to a termination or reference voltage slightly more negative than the desired logic LOW level, through a resistor whose value should



SHUNT TERMINATION

equal or slightly exceed the characteristic impedance of the transmission line. With this protocol, charging of the intrinsic line capacitance is very rapid, allowing the duration of rising and falling edge wavefronts to be maintained at a minimum. Primary wavefront reflections are almost totally damped by the terminator at the end of the transmission line; however, considerably more power is required for this protocol than by series termination, and a second supply voltage, the  $V_{TT}$  reference, is required.

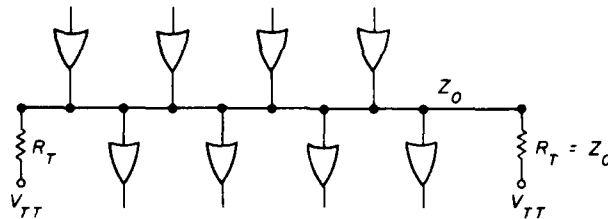
Finally, an unterminated transmission protocol could be used. In this protocol, considerable signal ringing occurs because the impinging wavefront reflects back and forth between the open circuited far end of the line and the low output impedance (approximately 7 ohms) of the source at the near end



UNTERMINATED TRANSMISSION

of the line; these reflections can continue through many round trip traversals of the interconnect. This protocol is strongly discouraged, and is, in fact, considered a design rule violation in system designs carried out at Mayo. The Mayo ECL CAD program described in Part II of this report will not permit an unterminated transmission line protocol.

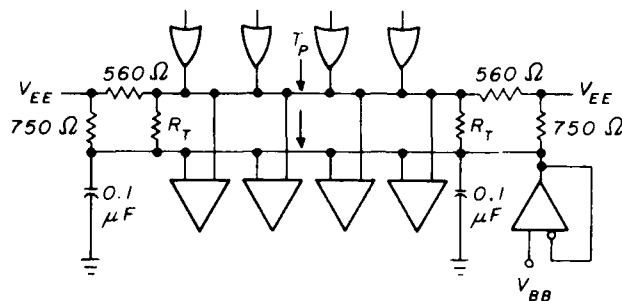
Of the various protocols described in the preceeding comments, the following studies always assume that the single ended protocol of choice is shunt termination, because of its speed and freedom from reflections. The requirement for the  $V_{TT}$  supply and the increased power consumption of this protocol are considered a worthwhile commitment of resources to achieve high speed signals nearly free of reflections. For differential signal transmission, the higher noise margins, greater reliability, and freedom from reflections of the single source, single destination transmission approach makes it the protocol of choice in comparison to the daisy chain interconnection method. For highest system reliability, party line and bus-



PARTY LINE OR BUS-ORIENTED TRANSMISSION

oriented protocols using the wire-or capability of subnanosecond ECL can be used on a single logic board (and are supported by the Mayo ECL CAD package) but should be used only as a last resort when the sources and destinations in a given party line circuit are on different logic panels. The data on which these statements are based will be presented in detail in Part I, Sections 4 and 6 of this report. For additional discussions

of transmission protocols, see Reference 3, Chapter 5.



### ALTERNATE DATA BUS TRANSMISSION PROTOCOL

### Selection of Wire Types for Intraboard Interconnects

Figure 12 represents a TDR study in which "single-ended" signal transmission with twisted pair wire (i.e., signal wire

### TIME DOMAIN REFLECTOMETRY CHARACTERIZATION OF TRANSMISSION LINES FOR SHORT RISETIME SINGLE-ENDED DIGITAL SIGNALS

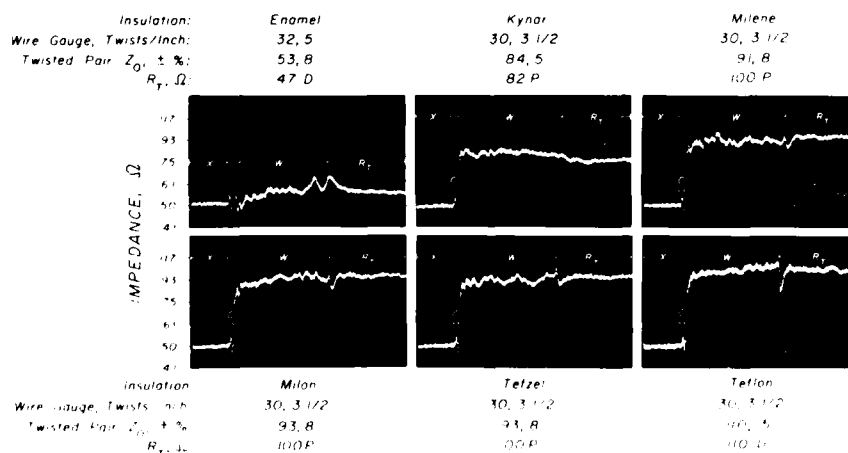


Figure 12

twisted with ground wire) of a variety of types and gauges was tested for transmission uniformity and interaction characteristics with a discrete or pack terminator matched to the line impedance. The #32 AWG enamel-covered wire possesses the lowest impedance but displays the largest percentage impedance nonuniformity and is physically fragile; hence it was removed from further consideration. The Teflon-insulated wire possesses the highest impedance and the shortest propagation delay per unit length of all materials examined (about five percent shorter than Kynar) but possesses undesirable cold flow properties. For all samples tested, impedance variations are apparent due to varying separation between the twisted pair transmission line and the ground plane (a phenomenon circumvented when stripline multilayer logic panels are employed) as well as to transmission nonuniformities ("modeing") in the twisted pair material itself. As indicated above, best overall system performance will be obtained by optimizing the interconnect protocol for minimum feasible transmission line impedance; the Kynar has a 25 percent lower characteristic impedance but is only five percent slower than the Teflon. Of equal significance is the percentage impedance variability of the interconnect material, since such variations generate small-amplitude distributed reflections which degrade rise/fall times. As a general "rule of thumb," the percentage voltage reflection expected from an impedance discontinuity is approximately half that of the percent impedance discontinuity. Worst case voltage reflections for the Kynar were on the order of  $\pm 3$  to 4 percent, i.e., less than the  $\pm 15$  percent

specified by the first-source component vendor as the maximum allowable to maintain acceptable noise margins (Reference 3). Similar results were observed for differential transmission schemes, with all average impedances five to ten percent greater than for the single-ended case (Figure 13).

TIME DOMAIN REFLECTOMETRY CHARACTERIZATION OF TRANSMISSION LINES  
FOR SHORT RISETIME DIFFERENTIAL DIGITAL SIGNALS

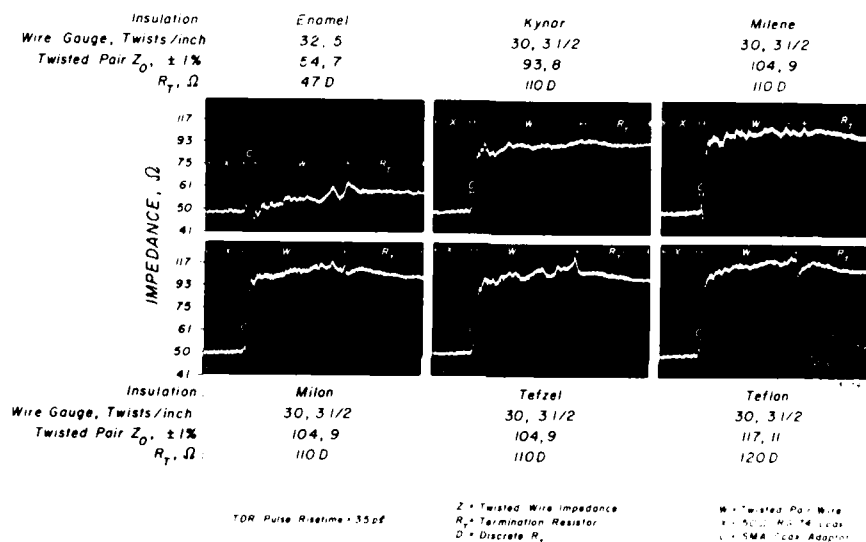


Figure 13

Operational Tests of Single Wire, Single Wire Twisted with Ground, Wire Wrappable Coax, and Semirigid Coax Interconnects and Their Contribution to On-Board Noise and Crosstalk

The use of twisted pairs for component-to-component interconnects has the following significant advantages in comparison



to single-wire signal runs. 1) Average impedances for a given wire gauge and insulation are 15-25 percent lower for the twisted pair approach than for single wires. 2) Impedance non-uniformities for twisted pairs are  $\pm 5$ -10 percent on average; conversely, impedance nonuniformities for single wire interconnects can in some instances approach  $\pm 20$  percent, resulting in wavefront reflections of large amplitude. 3) Crosstalk between sets of twisted wires is at least 3 dB lower than for single conductors.

Figures 14 and 15 illustrate the introduction of crosstalk into signal strings by the inductive and capacitive coupling effects of adjacent strings. The test circuit consisted of a driving gate and a length of Kynar-coated interconnect wire to the input of the second gate; the signal string was terminated to -2 V with a discrete 68 ohm resistor (a discrete resistor was used to preclude introduction of noise into the signal string by a terminator pack). The open input of the driving gate was held to a logic LOW level by its internal pulldown resistor. The output from the receiving gate was also terminated with a discrete 68 ohm resistor to -2 V. The test string was installed over an already existing circuit wiring mat for a system containing approximately 70 integrated circuits. Noise and crosstalk measurements were then performed, with the test string interconnect fabricated both with a single-conductor wire and with the single conductor twisted with a ground wire at 3.5 twists per inch. To generate a typical

level of background "noise", the 70-circuit system was operated at clock rates of 50 MHz and 125 MHz. Test string lengths of 12 and 25 cm were used, with noise measurements recorded at both the source and destination of the test string. Figure 14 demonstrates that at a clock rate of 50 MHz, for both the single conductor interconnect and a single conductor interconnect twisted with ground, the noise voltage peak-to-peak amplitude measured at the source was the same for both wiring protocols for the same lengths of interconnect wire. The left and right panels of the first and third rows of Figure 14,

Figure 14. Noise voltage (V) versus time (sec) for a 70-circuit system at 50 MHz. The left and right panels of the first and third rows of Figure 14 are identical. The left and right panels of the second and fourth rows are identical.

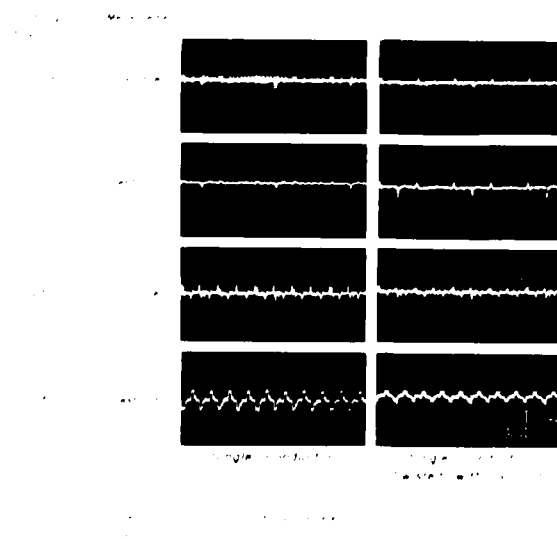


Figure 14

noise measurements recorded at the driving gate) indicate that the peak-to-peak crosstalk voltage was approximately the same but the noise power was slightly worse for the single wire interconnects. Conversely, the second row of images indicate that crosstalk measured at the destination was approximately the same, and of negligible magnitude, for a 12 cm string regardless of which wiring protocol was employed. However, for the 25 cm interconnect, peak-to-peak crosstalk measured at the destination was approximately twice as great for the single wire interconnect as for the twisted pair wire (i.e., 125 mV versus 60 mV peak-to-peak).

Figure 15 depicts similar measurements made with the 70-circuit system operating at a clock rate of 125 MHz. For the 12 cm test string length the crosstalk levels measured at both the source and destination were the same for the single wire and twisted pair interconnects, but the crosstalk measured at both the source and destination for the 25 cm interconnects was approximately 50% worse for a single wire interconnect than it was for the twisted pair interconnect (130 mV versus 80 mV peak-to-peak). These findings indicate that electromagnetically and electrostatically coupled crosstalk in short wires up to approximately 4 inches in length is small enough to negate differences between single wire and twisted pair interconnect protocols; however, for interconnects longer than 4 inches, a substantial improvement in crosstalk immunity can be gained with twisted pair interconnects. Considerable variability has been observed between crosstalk measurements made

CROSSTALK-INDUCED NOISE IN SUBNANOSECOND ECL  
CIRCUIT INTERCONNECTS FABRICATED WITH WIRE WRAP TECHNIQUES  
(125 MHz System Clock)

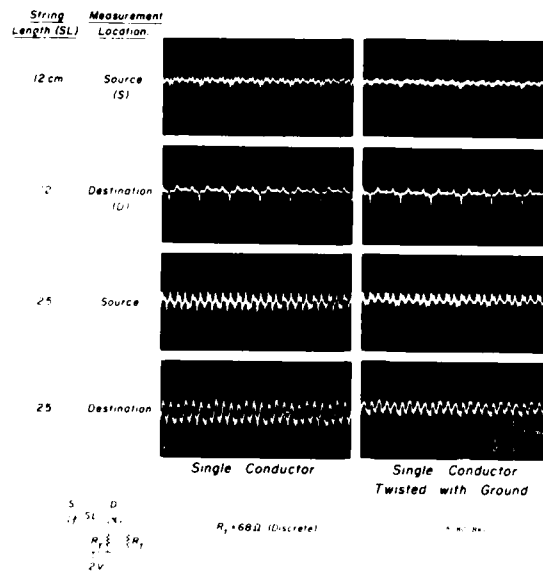


Figure 15

on different strings because of natural variations in layout and placement. As a result, signal-string crosstalk performance occasionally appears to violate predicted behavior; e.g., a long single wire may occasionally exhibit less crosstalk than a short twisted pair. On a statistical basis, however, the twisted pairs exhibit less crosstalk than single wires. Figure 16 is a photomicrograph of the backplane of Figure 11 wired with the twisted pair protocol described above.



Figure 16  
BASEPLANE OF A LARGE SUBNANOSECOND ECL LOGIC PAGE,  
WIRED WITH A TWISTED PAIR WIRING PROTOCOL.

## Crosstalk-Induced Parasitic Oscillations in Subnanosecond ECL Systems Caused by Packaging and Lead Dress Inadequacy

Because ECL integrated circuits are nonsaturating devices (some SSI single-gate part types can actually be operated as Class A amplifiers over a substantial part of their normal voltage excursion), they are somewhat more susceptible to oscillation than conventional TTL integrated circuits. In a manner similar to analog amplifiers, ECL gates can oscillate if a portion of the output signal is fed back to the input via magnetic or electrostatic coupling with a sufficiently large gain and a phase shift of  $180^\circ$  from output to input. Figure 17 demonstrates that such oscillations can indeed occur, although a considerable amount of contrivance was required. Clock signals appear to be most susceptible to this problem; oscillations in the clock strings are also those which can create the largest possible system disturbances. The upper left panel of Figure 17 shows that improper topologic layout of the clock string creates a growing oscillation on the logic HIGH level of the clock waveform which is rapidly damped on the logic LOW portion of the signal, as overall circuit string impedance alters when the output transistor is either fully conducting or nearly turned off (ECL transistors are never allowed either to saturate or undergo hard cutoff). The lower left panel shows the same clock waveform on a longer time scale; the oscillation builds up to a maximum of 150-250 mV peak-to-peak and then stabilizes. In general, the parasitic oscillation must initially be triggered

CROSSTALK-INDUCED PARASITIC OSCILLATIONS  
IN SUBNANOSECOND ECL CIRCUITS  
DUE TO PACKAGING AND LEAD DRESS INADEQUACY

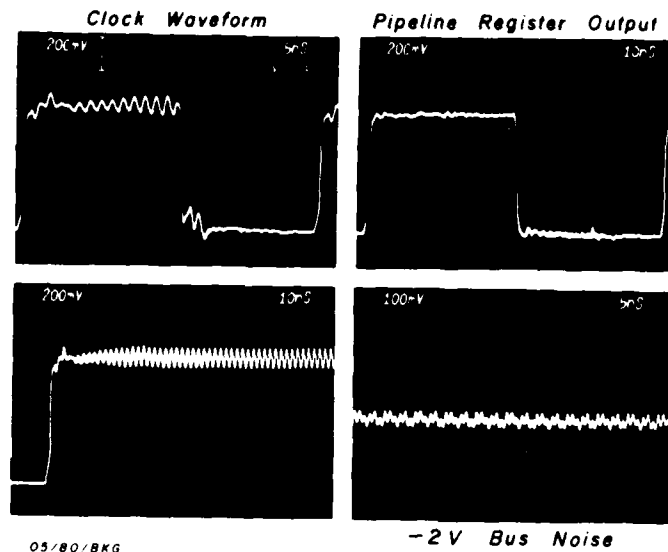


Figure 17

by a small amount of overshoot just following the rising edge of the waveform. The upper right panel of this figure indicates that the oscillatory behavior observed on the clock waveform does not propagate throughout the system, but is localized within single strings. These oscillations are always blocked by registers and hardly ever traverse gates elsewhere in the system. Clock waveform oscillation clearly degrades the noise margins of the signals so affected, and, as depicted in the lower right panel of this figure, can "leak" through into the

-2 V bus as well. It must be stated emphatically that the oscillatory behavior depicted in Figure 17 has never been observed in a circuit in which reasonable attention to layout protocols (i.e., no cabling of multiple wires in parallel channels, proper use of twisted pairs, correct signal string termination, and random runs of wire across the backplane) has been given. Furthermore, oscillation problems may readily be alleviated by rerouting the offending strings to follow different pathways across the backplane.



## Wavefront Dispersion Characteristics of Twisted Pair Interconnect Protocols

Although in general every attempt should be made to avoid long interconnect wires between individual components in a sub-nanosecond ECL circuit string, there are times when the topology of the circuit layout makes a few long interconnects unavoidable, particularly when a previously fabricated and optimized circuit board requires an engineering design change which includes the insertion of additional components into the board. As a result of energy losses via coupling to adjacent wires and signal pins, one would expect considerable degradation of the risetime of a high frequency signal with increasing length of the interconnect. The effective intercomponent propagation delay thus becomes the combined propagation delay through the interconnect and the degraded risetime of the wavefronts due to the dispersion losses. Figure 18 depicts measurements of the rising edges of a typical LOW-to-HIGH wavefront transition, for various lengths of single ended Kynar twisted pair interconnect terminated in its characteristic impedance. The upper leftmost image depicts the rising edge at the driver gate output; the remaining five panels depict the waveform rising edge at the terminator resistor for 5 cm, 10 cm, 20 cm, and 50 cm interconnect wires; the lower rightmost panel displays both the rising and falling edges of the pulse for the 50 cm interconnect. Rising and falling edge conformations are similar, but not identical, since the active ECL gate pulls its output logic signal

WAVEFRONT DISPERSION CHARACTERISTICS OF  
LONG TERMINATED INTERCONNECTS  
FABRICATED WITH WIRE WRAP TECHNIQUES  
(Drive Signal via Subnanosecond ECL Gate;  
Wiring Protocol: Signal Twisted with Ground; 30 AWG Kynar)

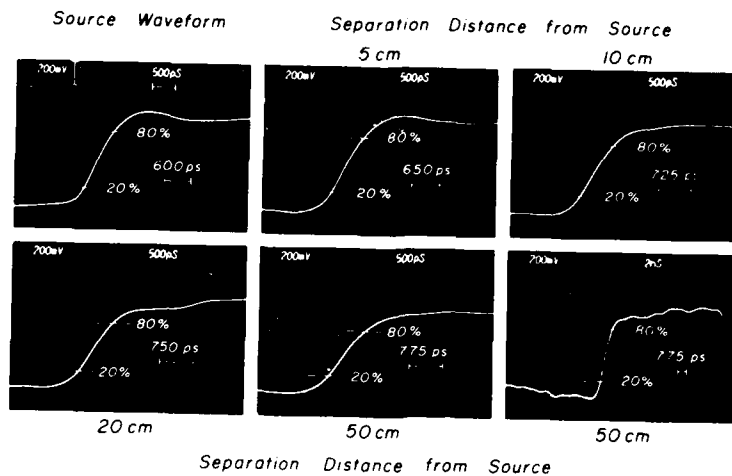


Figure 18

to the HIGH state, while the terminator pulls the logic signal to the LOW state when the gate becomes nonconducting. The 20-80% risetime of the waveform gradually lengthens from 600 psec at the source, to approximately 1.5 nsec at the destination end of the 50 cm interconnect. The results were unexpected: wavefront risetimes of twisted pair wire interconnects up to 50 cm in length are not seriously degraded, and, in general, do not cause problems except for circuits operating at the maximum feasible clock rate of subnanosecond ECL (i.e., above

250 MHz). However, as documented in Figures 14 and 15, interconnects of 50 cm should be avoided whenever possible because of their susceptibility to electromagnetically and electrostatically induced crosstalk. A similar series of measurements made for single wire interconnects of 5, 10, 20, and 50 cm revealed similar dispersion characteristics. However, the impedance nonuniformities of single wire interconnects are so large that they should be avoided for all but the shortest interconnects (2 inches or less).

#### Use of Wire Wrappable Coax for Backplane Interconnects on Large ECL Panels

The use of 50 ohm and 75 ohm wire wrappable coax (W. L. Gore, Inc., Part #CXN1213 and Part #CXN1233, respectively) for backplane interconnects in an ECL environment was investigated, using the same test jigs and protocols for noise, crosstalk, and operational performance employed for the twisted pair interconnects presented in the previous sections of this report. The wire wrappable coax was initially tested in late 1978, and found to be highly susceptible to short circuiting when the drain wire associated with the coax shield was separated from the body of the coax for wire wrapping. This unsatisfactory mechanical behavior was reported to W. L. Gore, Inc.; when the "same" wire was re-examined in early 1980, the mechanical instability of the material had been corrected.

Figure 19 demonstrates crosstalk measurements at the source and destination ends of a 20 cm length of 75 ohm wire wrappable coax. The input to the drive gate of the logic string under test was pulled down to -2 V; these crosstalk measurements were performed while a large system on the same logic panel was operating at clock rates of 50 and 125 MHz. Peak-to-peak crosstalk at the destination end of the 20 cm string was less than 30 mV, i.e., a lower crosstalk level than for a twisted pair wire run of the same length, as depicted in Figures 14 and 15. Although the crosstalk immunity of the wire wrappable coax at

**CROSSTALK-INDUCED NOISE IN  
SUBNANOSECOND ECL CIRCUIT INTERCONNECTS  
FABRICATED WITH 75  $\Omega$  WIRE-WRAPPABLE COAX**

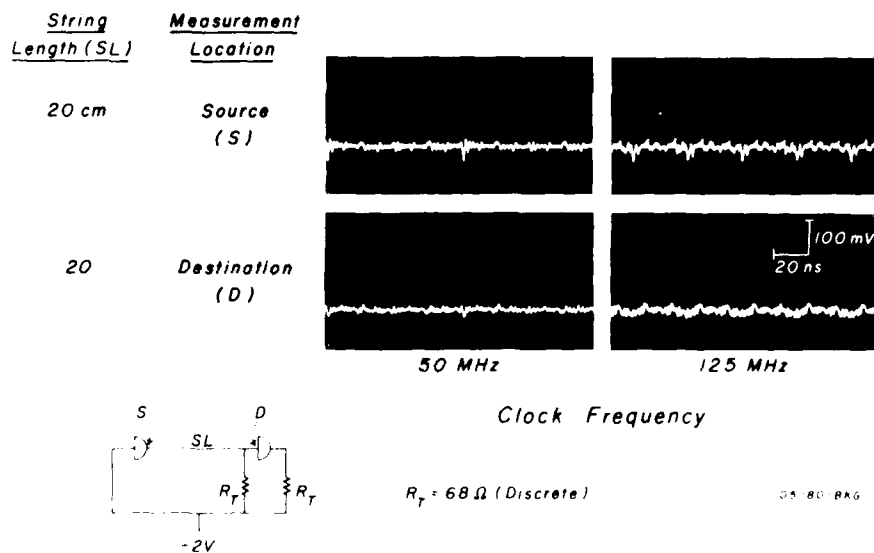


Figure 19

run lengths greater than 15-20 cm is superior to single-ended twisted pair by approximately 3-5 dB, the material is considerably more expensive, mechanically stiffer, and somewhat more difficult to install than twisted pair.

Figure 20 depicts operational measurements at clock rates of 50 MHz and 125 MHz in a four-node signal string fabricated with 75 ohm wire wrappable coax. In comparison with the

EFFECTS UPON WAVEFORM CONFORMATION OF  
SIGNAL STRING FABRICATION WITH 75  $\Omega$  WIRE WRAPPABLE COAX  
(ECL Dice Packaged in Ceramic Dual In-Line Packs,  
Signal String Composed of End Pairs Only)

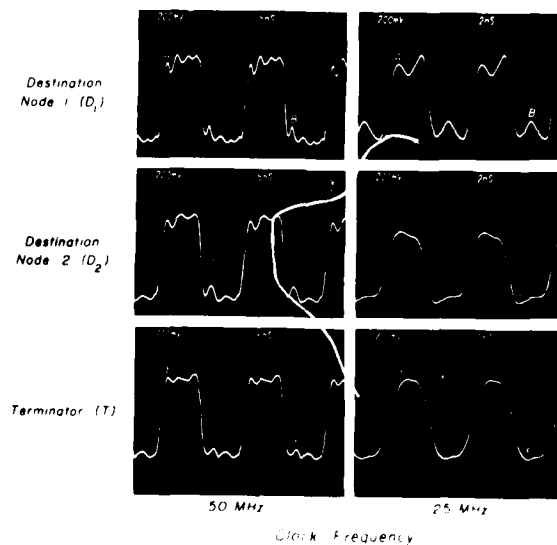


Figure 20

operational performance of semirigid coax (Figures 34, 35, and 36), the performance of the wire wrappable coax string is similar though not identical; these differences are observable in the conformation of the signals at the 125 MHz clock rate, due to the slightly higher wavefront dispersion and concomitantly slower risetimes of the wire wrappable coax. As may be seen at Letters A through F, the levels of overshoot and reflection following the rising and falling edges of the wavefronts are acceptable at both frequencies.

Although it would be cumbersome and unnecessary to fabricate an entire backplane with this material, it is an ideal transmission medium for the occasionally unavoidable long wire runs which cannot be removed by computer-aided optimization prior to board fabrication. In addition, engineering changes must frequently be carried out in a system prototyping environment after a board has already been optimized and fabricated. Long wire runs are often unavoidable in such cases as a result of shortages of empty socket locations in the vicinity of the design correction. The use of wire wrappable coax to support engineering design changes is an appropriate use of this material which maintains the stability and high noise immunity of the ECL system.

Wire wrappable coax can also be used to create the delays of a few nsec frequently required in the design of control circuits for ECL processors. Although active delay lines are

available commercially for subnanosecond ECL systems (EC<sup>2</sup>, Inc., is a vendor of such devices), the minimum delay available in these units is approximately 2.2 nsec  $\pm$  10%. If delays less than 2 nsec are required, or if delay tolerances less than  $\pm$  10% are mandatory, a section of wire-wrappable coax cut to the appropriate length will serve as a delay line with precisely tunable and very stable delay characteristics, exhibiting high noise and crosstalk immunity.

### Special Considerations in the Design of Pack Terminators

When multiple terminator resistors are incorporated into a single terminator package, one end of each resistor is generally connected to a small internal bus on the terminator substrate, which is in turn connected at one or more locations through socket pins to the -2 V supply (see the uppermost terminator pack in Figure 7). When large instantaneous amounts of current are pulled through one or more of the terminator resistors as their associated signal strings rapidly switch logic levels, self-inductance effects of this small internal bus cause its instantaneous voltage to fluctuate markedly from the nominal value of -2 V; every resistor and hence every logic string attached to the terminator pack manifests this change in reference bus voltage in the form of "terminator generated crosstalk". The "noise" which is apparent in the measurements from the early test jig circuits depicted in Figures 1, 2, 4, 5, and 6 was caused in part by terminator-induced crosstalk, since commercially available terminator networks are not properly designed to minimize this problem. It was thus necessary for us to design a terminator pack resistor containing an on-pack high frequency chip capacitor to decouple the terminator pack internal bus to ground. The upper leftmost component in Figure 7 is one of three 12-pin resistor network part types developed for this project. Pin 1 is on the left edge of the components. An internal supply bus runs along the upper edge of the ceramic substrate, with connections to the -2 V power



supply bus at pins 1 and 12. The nine small black squares are the 85 ohm,  $\pm 2\%$  tolerance CERMIT resistor elements; a small 3900 pF NPO chip capacitor is soldered at its upper end to the internal bus and at its lower end to pin 7. It was discovered that all types of miniature chip capacitor are not electrically equivalent at very high operating frequencies. With assistance from Murata Corporation of America, we investigated the electrical properties of various synthetic dielectric materials used in chip capacitors, including NPO, BX, X7R, and Z5U dielectrics. Of these, only the NPO-based capacitors demonstrate low impedance at frequencies above 100 MHz. Hence, these more expensive devices are used, not because of their well known temperature stability, but because of their superior high frequency performance.

Careful selection of terminator resistor characteristics can have a major impact on the performance of ECL signal strings. Two factors must be considered in the selection of terminator characteristics. First, the impedance of the terminator resistor should equal or slightly exceed the average impedance of the transmission line. As discussed later in this report, terminator impedances less than the line impedance create wavefront reflections with a polarity toward the logic threshold, thus decreasing logic signal noise margins; terminators exactly matched to the line impedance cause no reflections whatsoever; terminators whose impedance exceeds that of the line cause positive wavefront reflections, i.e., in the polarity direction away from

threshold, which do not decrease system noise margins. Hence, terminator impedance values should never be less than the line impedance. The single ended twisted pair wiring protocol developed in this research has a characteristic impedance of approximately 75 ohms. The impedance of the 85 ohm resistor networks is actually 75-80 ohms as a result of unavoidable shunt capacitive reactances of a fraction of a picofarad introduced by the physical structure of the terminator network. The non-pure-real nature of the terminator network does create a small amount of phase offset between voltage and current waveforms on the transmission line, but less than that caused by the several pF shunt capacitance introduced by the integrated circuits themselves (see the discussions of integrated circuit capacitive loading of the ECL signal strings in Section 5 of this report). As documented in Figure 12, these terminators provide a good match of average line impedance in the twisted pair backplane environment.

The second important consideration in the design of terminator networks is the percent tolerance of the resistor values to be employed. Since a primary function of the terminator is to prevent voltage wavefront reflections from propagating back along the transmission line, the following equations reveal an interesting tradeoff between average transmission line impedance and percent tolerance of the terminator network values (Reference 3). The magnitude of the wavefront reflection from the terminated end of a transmission line is related to the closeness of the match between the terminator resistor  $R_T$  and the

line impedance  $Z_o$ . The ratio of the reflected voltage  $V_r$  to the incident voltage  $V_i$  is the reflection coefficient  $\rho$ , i.e.,

$$\rho = \frac{V_r}{V_i} = \frac{R_T - Z_o}{R_T + Z_o}$$

This equation can be rearranged into a form which allows an assessment of the permissible range of  $R_T$  and  $Z_o$  if the maximum permissible voltage reflection is known from other data:

$$\frac{R_T}{Z_o} = \frac{1 + \rho}{1 - \rho}$$

Since the first-source vendor of ECL 100K states that  $\rho$ , the ratio  $V_r/V_i$ , should not exceed  $\pm 15\%$  if system stability is to be assumed, the following bounds may be established:

$$\frac{1.15}{.85} > \frac{R_T}{Z_o} > \frac{.85}{1.15}$$

Stated alternately, the tighter the limits on  $R_T$ , the looser the limits on  $Z_o$  may be, and conversely. However, the tolerance of  $Z_o$ , the line impedance of the twisted pair wire in a wire wrap environment, simply cannot be tightly controlled. Hence, the tolerance of  $R_T$  should be tightly controlled to compensate for unavoidable variations in  $Z_o$ .  $R_T$  tolerances

of  $\pm 10\%$  allow  $Z_0$  tolerances of  $+22\%$ ,  $-19\%$ ;  $R_T$  tolerances of  $\pm 5\%$  allow  $Z_0$  tolerances of  $+28\%$ ,  $-23\%$ ;  $R_T$  tolerances of  $\pm 2\%$  allow  $Z_0$  tolerances of  $+32\%$ ,  $-24.5\%$ ;  $R_T$  tolerances of  $\pm 1\%$  allow  $Z_0$  tolerances of  $+34\%$ ,  $-25.2\%$ . Based upon steadily increasing costs for the tighter tolerance resistor values, our analysis indicated that  $R_T$  tolerances of  $\pm 2\%$  were the optimum selection.

The resistor network displayed immediately below the locally decoupled terminator pack in Figure 7 also contains an internal bus connected to pins 1 and 12, but contains ten  $470\text{ ohm} \pm 2\%$  CERMIT resistors and no decoupling capacitor. This resistor pack contains "pull down" resistors used at the differential output pins of driving gates to supply a constant pull-down current and LOW reference voltage to allow the differential driving gates to switch rapidly. Since the resistance values of these CERMIT resistors are much higher than the line impedance, and since they are connected to  $-4.5\text{ V}$  ( $V_{EE}$ ), each tends to function as a low level constant current source, and hence on-board decoupling capacitors are less necessary. The third resistor network from the top in Figure 7 contains six individual  $100\text{ ohm} \pm 2\%$  resistors, each of which is connected between the  $Q$  and  $\bar{Q}$  lines in a differential transmission line protocol. The lower leftmost component in Figure 7 indicates the appearance of the terminator packs with the ceramic encapsulation in place.

## Noise Induced Into Operating Signal Strings Through Pack Terminators

In order to test the amount of crosstalk introduced into operating signal strings by the terminator packages of Figure 7, a series of crosstalk experiments were carried out using both discrete terminator and pack terminator resistors.

Measurements were made of the high frequency noise in a test signal string with a standard ECL driver gate as the source, and a length of 1.5 inches of "single rail" twisted pair interconnect line (i.e., signal wire twisted with ground wire), terminated with a discrete 68 ohm resistor to -2 V. The interconnect wire between source and destination was deliberately made very short to minimize the amount of noise induced into the test string by electromagnetic and electrostatic coupling through the wires themselves (the usual route for crosstalk-induced noise). Measurements of the signal waveform were made at the output pin of the driver gate (test point "A") and at the terminator resistor (test point "B"). The test string was positioned on the wiring net of an operating 70 component system, which latter was then operated at 50 MHz and 150 MHz clock rates. In several experiments, the source gate for the test string was also driven by a clock signal; two different clock phases, offset from one another by 90°, were used to drive the test string and the 70-circuit system to further randomize the noise superimposed on the test string. The upper row of

Figure 21 depicts measurements at a clock rate of 50 MHz; the upper leftmost two waveforms were recorded at points A and B respectively. The upper rightmost panel represents the cross-talk recorded with the clock input to the test circuit driver set high or either a logic HIGH or a logic LOW level (since the cross-talk levels were the same for the logic HIGH and logic LOW values, only one trace is shown). The lower row of panels show the results of similar measurements recorded when both the test circuit and the background circuit were operated at a clock rate of 100 MHz, but with a timing phase offset between

MEASUREMENT OF CROSS-TALK NOISE IN  
SUBNANOSECOND LOGIC STRINGS THROUGH DISCRETE TERMINATION  
Fully Replicated Logic Panels persisting at Clock Input Frequency

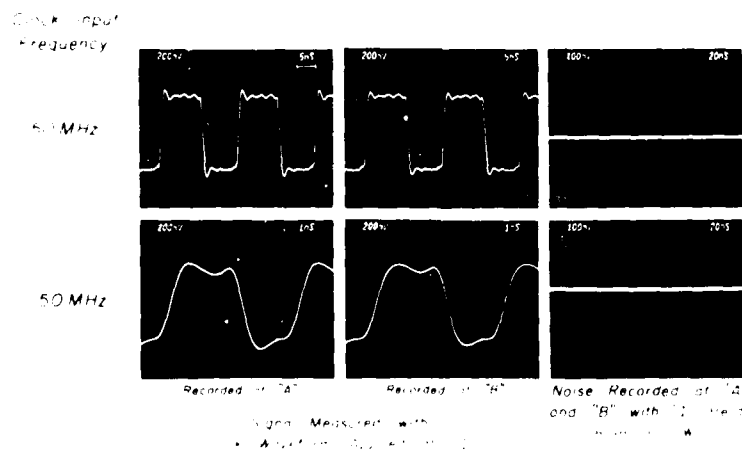


Figure 21

the clock waveforms used to drive the main circuit and the test string. Again, the peak-to-peak crosstalk measured at this higher clock rate was negligible.

Figure 22 shows the results of similar measurements made at a 50 MHz clock rate, with the test string terminated with one of the resistors in a capacitor-decoupled terminator pack. The upper row of images records noise measurements from point A in the test string with the input to the test gate driven by the clock signal (leftmost panel), with the input to the test gate held in the logic LOW state (middle panel), and with

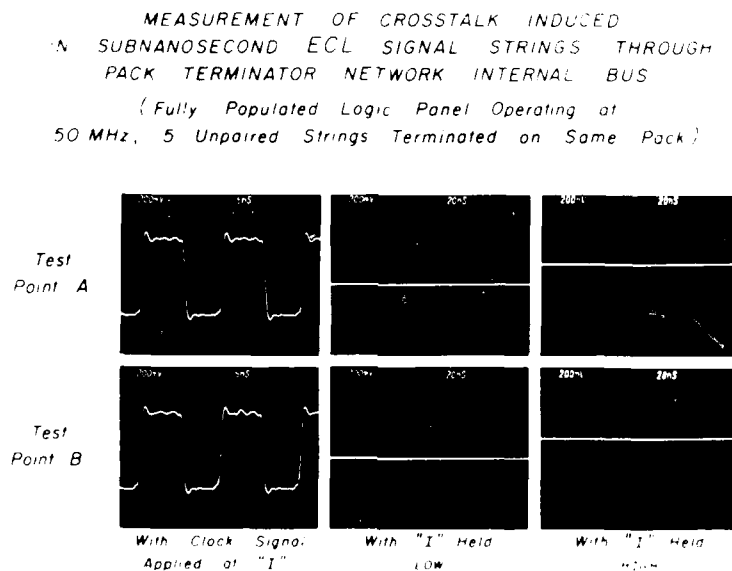


Figure 22

the input to the test gate is in the high state (upper panel). In the lowermost row of figures, the same measurements were repeated with the test probe positioned at point B. In all cases in Figure 22, four other operating signal strings were terminated to other resistors in the same terminator pack; however, care was taken to assure that these other four strings were not true/complement pairs from the same driving gates. Figure 23 depicts a similar set of results from the same test circuit arrangement, but with a system clock rate of 150 MHz. For the experiment whose results are depicted

MEASUREMENT OF CROSSTALK  
INDUCED IN SUBNANOSECOND-LEVEL SIGNAL STRINGS THROUGH  
PACK TERMINATOR NETWORK INTERNAL BUS  
Fully Populated Logic Plane Operating at 150 MHz,  
5 Unpaired Strings Terminated (on Same Pack)

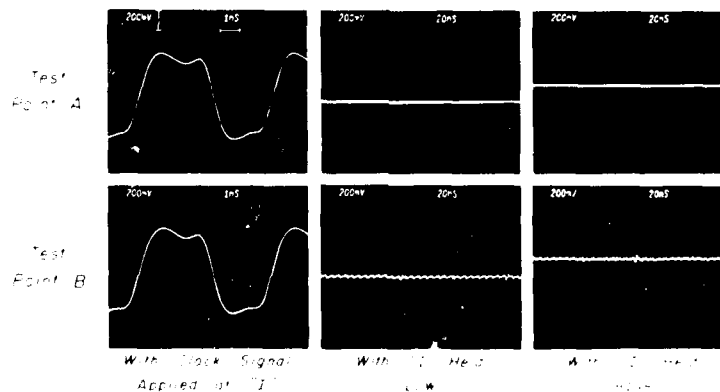


Figure 23



MEASUREMENT OF CROSSTALK INDUCED  
IN SUBNANOSECOND ECL SIGNAL STRINGS THROUGH  
PACK TERMINATOR NETWORK INTERNAL BUS  
(Fully Populated Logic Panel Operating at 50 MHz;  
4 Complement Pairs plus Test Circuit Terminated on Same Pack)

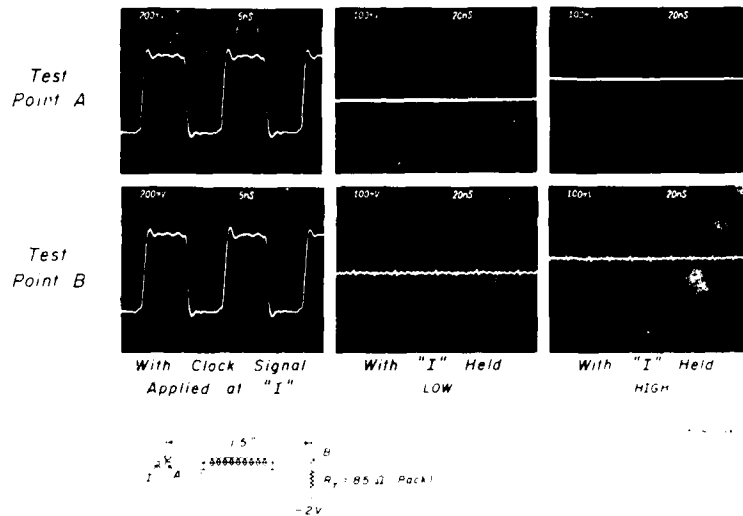


Figure 24

in Figures 24 and 25, the circuit strings were rearranged so that a total of nine signal strings would be terminated on the same resistor pack, including the circuit string under test, and four pairs of true and complement drives from four separate driving gates from the 70-integrated circuit background system.

A thorough analysis of the results depicted in Figures 21 through 25 has yielded a comprehensive set of design rules for the use of capacitor-decoupled terminator packs and discrete

MEASUREMENT OF CROSSTALK INDUCED IN SUBNANOSECOND ECL  
SIGNAL STRINGS THROUGH PACK TERMINATOR NETWORK INTERNAL BUS

(Fully Populated Logic Panel Operating at 150 MHz;  
4 Complement Pairs plus Test Circuit Terminated on Same Pack)

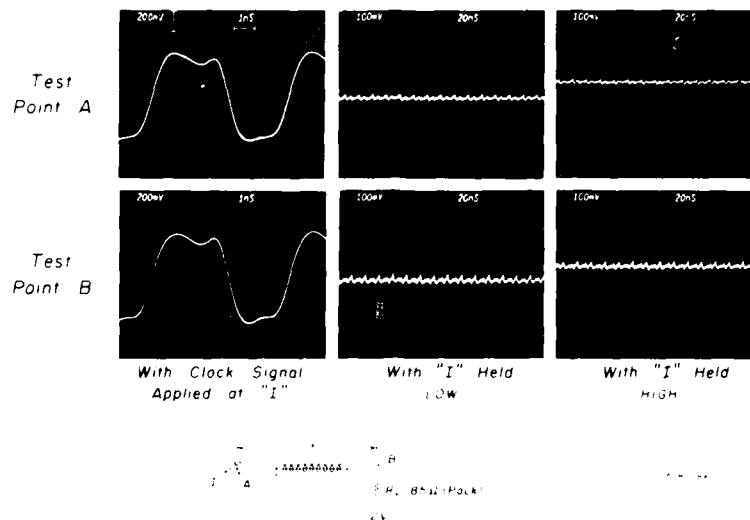


Figure 25

terminator resistors over a wide range of frequencies, which are summarized in the following eight rules: 1) Discrete resistor terminator-induced noise is no greater at high frequencies than at low frequencies. 2) If resistor networks include appropriate internal decoupling, noise induced through the terminator packs into signal strings is usually, though not always, slightly greater at high frequencies than at low frequencies. 3) Terminator pack-induced noise is similar or slightly smaller in amplitude at the source as at the destination. 4) The peak-to-peak noise amplitude in a signal string increases roughly linearly as the total number of signal strings

terminated on the same pack increases; in the examples examined, noise increased from 30 mV peak-to-peak with five strings terminated on the same pack to approximately 70 mV peak-to-peak with nine strings terminated on the same pack. 5) No decrease in terminator-induced noise can be achieved by connecting true and complement sides of the same driving gate to the same terminator pack (this result was unexpected, since it was assumed that a balanced current drain within the terminator would reduce overall noise). As a result, wiring protocols need not assure that true and complement sides of the same driving gate be terminated on the same terminator pack. 6) In order to minimize the level of instantaneous return path currents flowing in the ground and power planes of the logic board, any logic gate, flip flop, or other component possessing both true and complement outputs used in a design must be netted in the following specific manner. If one of the paired outputs from such a gate is used in the logical design as the source in a signal string, the other output of the true-complement pair must also be terminated to  $V_{TT}$ . If this other output is not required in the logical design, a "termination string" must nonetheless be created for it, though the true and complement terminator resistors need not be in the same terminator pack. As a corollary to this rule, device types which do not have true and complement output pairs should be avoided for the fastest systems, since the unbalanced AC ground return path currents so created will cause an increase in the levels of ground and power plane noise voltages. The severity of the noise introduced by unbalanced current flows becomes clear when it is

recognized that the series inductance of a 3 oz copper foil several tenths of an inch in width is 3-5 nanohenries per inch. The voltage drop per inch in such a foil for an ECL signal current from a single gate driving a 50 ohm load (15 milliamps) for a 1 GHz component of the subnanosecond signal wavefront is approximately 475 mV. Instantaneous voltage differences between two points on an AC ground plane one inch apart of such a large magnitude would markedly degrade system noise margins. Thus it is imperative to balance the average AC return path currents to the maximum possible extent by terminating true and complement outputs of all gates used in the design. 7) The peak-to-peak noise on a logic HIGH signal is no different from the peak-to-peak noise on a logic LOW signal. 8) Examination of signals in these experiments indicates that for a given clock frequency, the waveshape conformation is unaltered regardless of whether a discrete resistor or a properly designed terminator pack is used. It must be emphasized, however, that a properly designed terminator pack must be employed, as will be demonstrated unequivocally in Figure 26 (following section).

#### Measurements of System Noise at Several Critical Locations in an Operational Circuit

Figure 26 depicts measurements of system noise at several critical locations in a multicomponent test circuit fabricated with the logic boards, components, and wiring protocols described

above. The circuit was clocked at a 250 MHz rate for this series of measurements; all integrated circuits were verified to be operating correctly before the noise measurements were undertaken. The rightmost column of panels depict the internal bus noise of a standard terminator pack resistor network with decoupling capacitor in place, carried out by probing several packs which were manufactured without the final ceramic encapsulation layer. The upper rightmost image shows that with several randomly selected strings terminated to the resistor pack, the peak-to-peak noise measured on the terminator pack internal bus 2.5 mm from the decoupling chip capacitor is approximately 30 mV peak-to-peak; terminator pack internal

NOISE WAVEFORMS AT SELECTED LOCATIONS IN  
SUBNANOSECOND EMITTER COUPLED LOGIC(ECL) TEST CIRCUIT  
(250 MHz System Clock Generated via  
Square-Wave Oscillator; Interconnects via Wire Wrap)

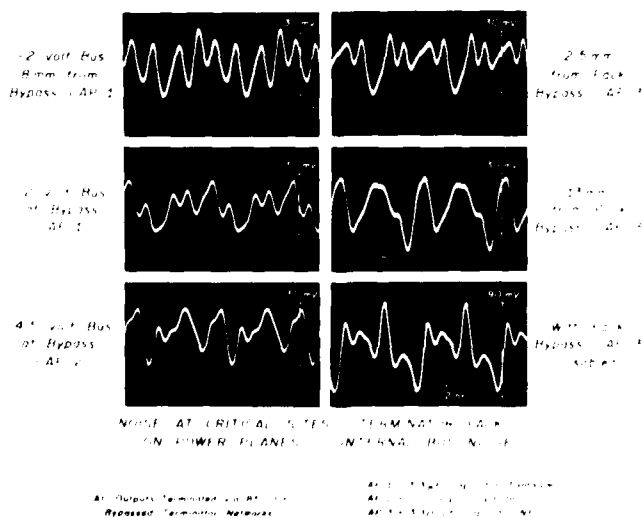


Figure 26

bus noise 13 mm from this decoupling capacitor is approximately 35 mV peak-to-peak, probably as a result of small differences in local instantaneous terminator bus voltage caused by the self-inductance of the terminator bus itself. The lower right-most panel in Figure 26 displays the internal bus noise following physical removal of the on-pack decoupling capacitor. Peak-to-peak noise was 90-100 mV, indicating that the internal decoupling capacitor decreases terminator pack-induced crosstalk between signal strings by at least a factor of three. Noise measurements made at two locations on the critical -2 V power plane (critical because this bus is the reference for the logic LOW level and cannot be voltage-compensated by the integrated circuits) are presented, as is one measurement from the - 4.5 V plane (this plane is less critical since the 100K ECL components have built-in on-chip compensation for the - 4.5 V supply). Note that for all power plane noise measurements, the peak-to-peak noise is less than 35 mV.

## SECTION 5

### EFFECTS OF INTEGRATED CIRCUIT PACKAGE IMPEDANCE DISCONTINUITIES UPON SIGNAL STRING INTEGRITY AND WAVEFORM CONFORMATION

The noise and crosstalk measurements described in the prior sections of this report indicated that subnanosecond ECL systems fabricated with the Mayo-developed components and wiring protocols should be able to operate at very high clock rates. To verify this hypothesis, a small prototype test circuit was fabricated using the specially designed wire wrapped subnanosecond ECL logic panel and components depicted in Figures 7 and 10. The prototype circuit (Figure 27) consisted of a clocked D-type

#### *PROTOTYPE DIGITAL CIRCUIT FOR INTEGRATED TEST OF SUBNANOSECOND ECL COMPONENTS, LOGIC PANEL, AND INTERCONNECT PROTOCOL*

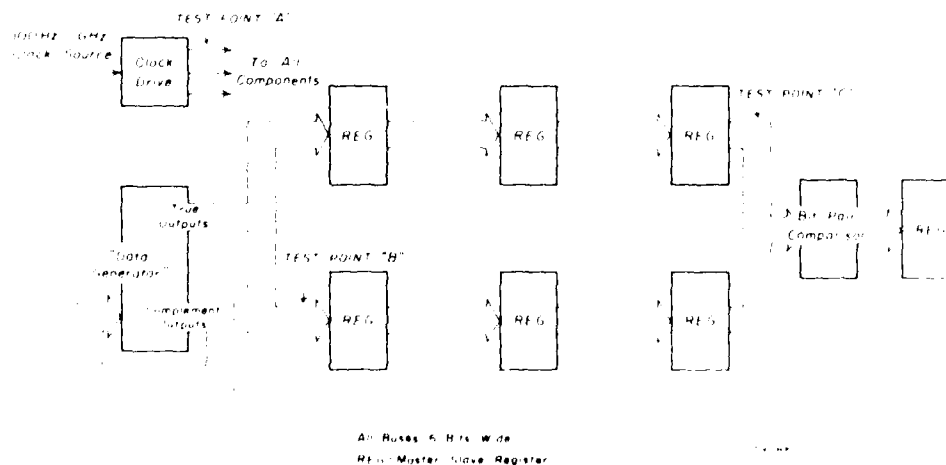


Figure 27

master-slave register whose inputs were each fed from the complement output of the same bit position. The output "data" from this "data generator" were then placed through two parallel banks of data registers; each pair of identical data were then compared in a bank of exclusive-or gates. Each bank consisted of three consecutive registers, thereby simulating the intermediate stages in a pipelined processor. The "data generator" and all registers were driven by a 250 MHz clock waveform from a commercial square wave pulse generator.

OPERATION OF PR. TYPE SYN. HANDED EX. AL. IN 1987  
 FABRICATED WITH SUBNANOSECOND Emitter-Coupled Logic (ECL)  
 250 MHz System Clock Generated via Square Wave  
 Oscillator, Interconnects via Wire Wrap

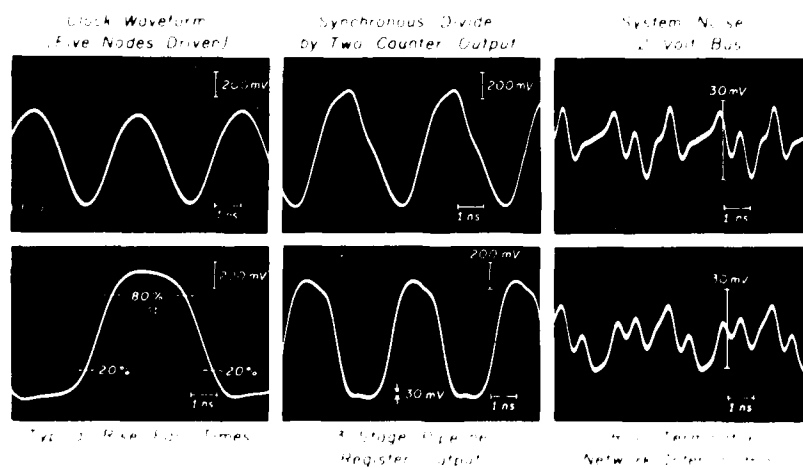
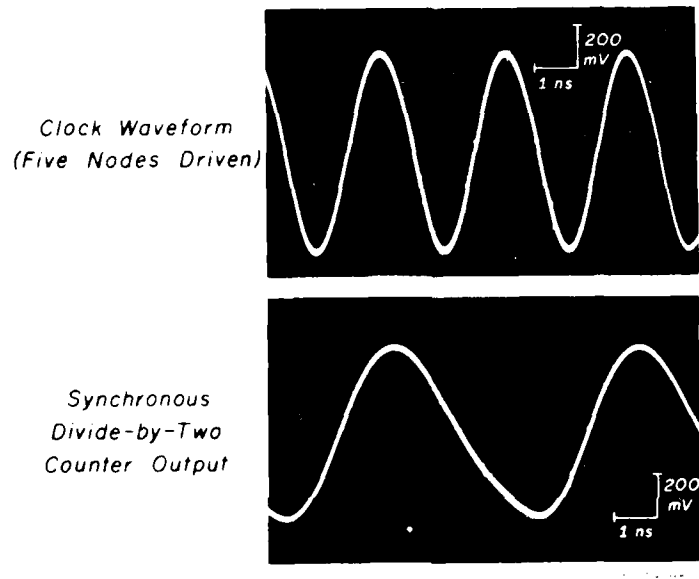


Figure 1. Clock and Divide by Two Waveforms



The lower left panel of Figure 28 depicts rising/falling edge wavefronts of a typical signal string in this test circuit which contained one source and three destination nodes; this panel demonstrates that rise/fall times were maintained at less than 1 nsec. The upper left panel depicts the 250 MHz clock waveform (measured at test point "A" in Figure 27), which appears sinusoidal because of bandwidth limitations of the oscilloscope and probe employed in these measurements. The middle panel in the upper row depicts one bit of the output from the "data generator" (test point "B" in Figure 27), while the middle panel in the lower row depicts one bit from a third stage register (test point "C" in Figure 27); both middle panels demonstrate proper operation of the prototype circuit (i.e., no missing transitions) at the 250 MHz clock rate. The rightmost panel of Figure 28 are records of system noise on the -2 V plane at pin 1 of the 85 ohm capacitor-decoupled terminator network, and on the internal bus of one of the same networks (upper leftmost component in Figure 7). These measurements confirm results already reported for Figure 26, that peak-to-peak noise at critical circuit locations is constrained to less than 30 mV (note the 30 mV amplitude marker on the lower center panel of Figure 28). This circuit operated with good performance margins at the 250 MHz system clock rate; however, as the clock rate was increased toward 400 MHz, various portions of the circuit gradually ceased operation. Figure 29 shows the clock waveform and the output of the data generator (test point "B" in Figure 27) operating at a clock rate of 350 MHz; however, performance of this circuit

OPERATION OF PROTOTYPE SYNCHRONOUS  
DIGITAL CIRCUIT FABRICATED WITH  
SUBNANOSECOND EMITTER COUPLED LOGIC (ECL)  
(350 MHz System Clock Generated via  
Square Wave Oscillator; Interconnects via Wire Wrap)



*All outputs terminated, via matched resistor, to input networks.*

Figure 29

at the 350 MHz clock rate was unreliable. These and other measurements indicated that clock rates of 350 MHz can be employed only for very small systems consisting of a few dual in-line packages, with system malfunction virtually guaranteed at frequencies greater than 350 MHz.

These upper limit clock rates of 350 MHz are in contradiction to published maximum ratings of 550 MHz for many subnanosecond ECL gates and MSI components, e.g., 8-bit master slave registers (Reference 3). To ascertain the reason for the degraded performance of these components, two different portions of the same test circuit were driven with two different phases of the same clock signal in such a manner that the clock phases could be shifted with respect to one another in increments of 10 psec. These studies indicated that the integrated circuits ceased performance at clock rates above 300 MHz because stable waveforms were not being established at the inputs of clocked registers sufficiently early to satisfy the setup constraints of the integrated circuit components. This was a puzzling result, since the design had been executed to guarantee that the setup time constraints would be achieved in all sections of the test circuit at least to clock rates of 500 MHz. It was finally recognized that the violation of the setup time constraints was caused by significant waveform distortions resulting from the propagation of wavefront reflections back and forth on each signal string. However, time domain reflectometry measurements of terminated signal strings without integrated circuit components in place indicated that the reflections did not originate from the transmission line terminator, but from secondary sites along the signal strings co-located with the integrated circuit pins connected to the signal string.

# Characterization of Typical Signal String Interconnect Structures Via Time Domain Reflectometry

Figure 30 depicts the impedance characteristics of a three-node signal string fabricated with single-ended twisted pair wire (leftmost panels), and the same string fabricated with 70 ohm semirigid coaxial cable (Uniform Tube, Inc., Part #ST41-70) soldered to the ground plane of the wire wrap board (rightmost panels). In the upper two panels, time domain reflectometry measurements were carried out on the signal strings with

## EFFECTS OF DIGITAL INTEGRATED CIRCUIT INPUT CAPACITANCES UPON IMPEDANCE CHARACTERISTICS OF MULTIPLE NODE SIGNAL STRINGS

(Measurements by Time Domain Reflectometry;  
 CERNIP\* Subnanosecond ECL Components)

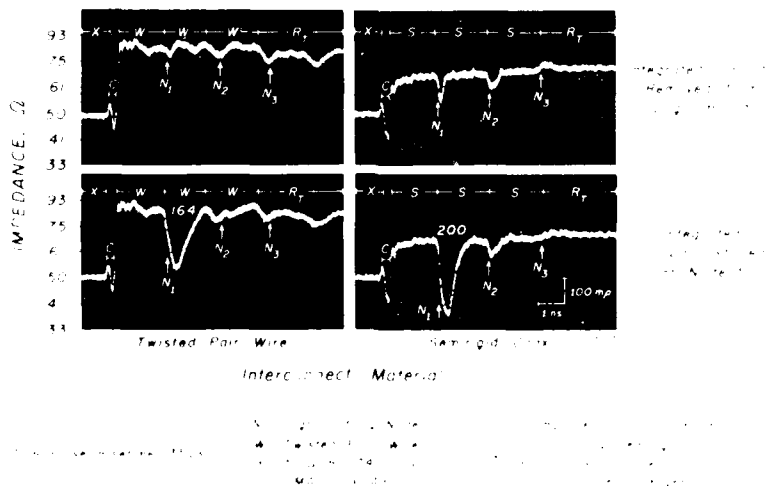


Figure 30

integrated circuit packages installed. Some impedance non-uniformity is evident in the signal string fabricated with wire wrap (leftmost panel), although the impedance discontinuities at the wire wrap pin nodes (indicated by the arrows and  $N_i$ ), are not as large as was originally expected. In the right upper panel, the local impedance variations between the nodes are relatively small, indicating good quality of the semirigid coax if handled with care. However, at the nodes, the impedance discontinuities are larger than for the wire wrap interconnects. It now appears that the process of soldering the central conductor of the semirigid coax to the integrated circuit socket pins causes a local thermally induced distortion of the insulating layer between the center conductor and the shield of the semirigid coax, extending into the body of the coax for 1 to 2 cm from the point of attachment of the center conductor. This results in a 1-2 cm impedance discontinuity in the approaching cable and a similar impedance discontinuity in the departing cable at each node; the round trip impedance discontinuity is several hundred psec in duration. These findings indicate that the expensive semirigid coax, while more uniform in the internode spacing than twisted pair wire, creates impedance discontinuities which to a small extent degrade overall system performance.

The lower two panels of Figure 30 depict several significant characteristics of the subnanosecond ECL integrated circuits. In both lower panels, an integrated circuit packaged

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MAYO CLINIC ROCHESTER MINN  
COMPUTER AIDED WIREWRAP INTERCONNECT.(U)  
NOV 80 B K GILBERT

F/6 9/5

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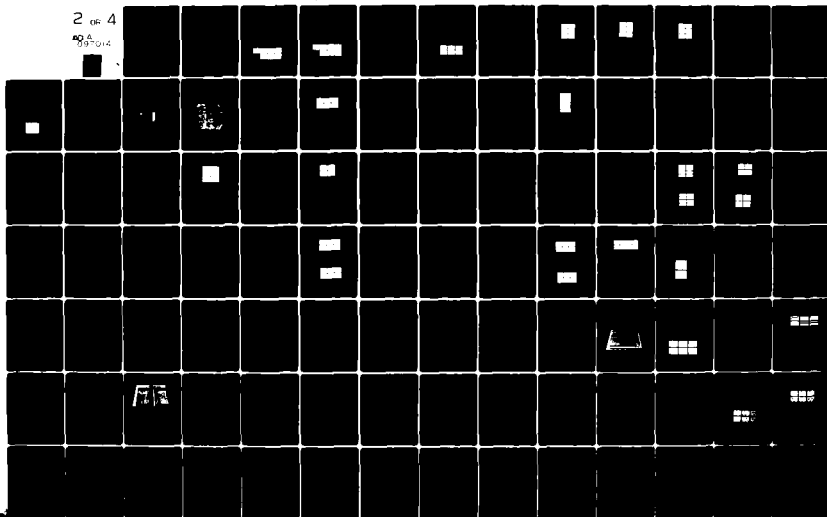
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in a 24 pin ceramic dual in-line (CERDIP) encapsulation was inserted into the node 1 position of each signal string. In the lower left panel, the connection point corresponded to a center pin on the CERDIP, while in the lower right panel, the connection point corresponded to an end pin on the CERDIP. A large impedance discontinuity is evident at node 1 in both lower panels. A rough "rule of thumb" indicates that the round trip duration of the discontinuity measured by the TDR will be identical to that observed in the operating circuit, while the magnitude of the reflection caused by the discontinuity will be roughly half the percentage impedance discontinuity observed in the TDR measurement. In the lower left panel of Figure 30, the impedance discontinuity magnitude is approximately 40% for a center pin on the CERDIP, while the impedance discontinuity magnitude (lower right panel) for an end pin on the CERDIP is approximately 50%, resulting in a voltage reflection for the center pin of approximately 20% and for an end pin approximately of 25%. Since the impedance discontinuity magnitude is less than the characteristic impedance of the transmission line, all voltage reflections will be "negative", i.e., a rising edge reflects as a falling edge, and vice versa. Negative reflections thus drive the instantaneous signal voltage toward the logic threshold of the gate, thereby decreasing the effective noise margin of the operating circuit. Based upon AC load line characteristics of the subnanosecond ECL family, the first-source vendor specifies that voltage upsets in the direction of the logic threshold from all causes combined shall not exceed

15% of the total signal swing if the speed performance and noise immunity of the logic family are to be maintained (Reference 3). As documented in Figure 30, in quite typical cases, the integrated circuit packages can themselves cause reflections whose combined amplitudes may equal or exceed the vendor-specified 15% limit.

The data of Figure 30 was shared with the first-source component vendor, who carried out further testing in his own facilities. Although expecting to measure approximately 2 pF shunt capacitance at the input pin of each gate, the vendor actually recorded input shunt capacitances to center pins of the Cerdip packages of approximately 5 pF, and shunt input capacitances to end pins in the range of 8-10 pF. These high shunt input capacitances are now attributed to the physical conformation of the large metal lead frame structure of the ceramic dual in-line packages, as well as the high dielectric constant characteristics of the ceramic encapsulation and its associated epoxy-bond material. As a result of these measurements, the first-source vendor packaged and sent to us a selected sample of subnanosecond ECL dice encapsulated in a newly designed plastic dual in-line package with a modified lead-frame structure and an integral heat sink, in an attempt to achieve lower input shunt capacitance.



# TDR Comparison Tests of Plastic DIP-Encapsulated and Ceramic DIP-Encapsulated ECL Dice

Figures 31 and 32 show the results of TDR measurements carried out in the Mayo facilities on plastic-encapsulated and Cerdip-encapsulated subnanosecond ECL dice, using a subtraction technique to isolate the impedance discontinuities caused by the integrated circuit and its package. Figure 31 depicts measurements for center pins on the plastic and ceramic dual in-line packages, while Figure 32 displays similar data for end pins. The upper leftmost images in both figures depict the baseline impedance characteristics of the signal strings with

## *EFFECT OF INTEGRATED CIRCUIT AND PACKAGE INPUT CAPACITANCES UPON IMPEDANCE OF MULTI-NODE SIGNAL STRING (Measurements by Time Domain Reflectometry, Subnanosecond ECL ICs in Plastic and Cerdip Packages, Interconnects via 70Ω Semirigid Coax, Package Center Pins Tested Only)*

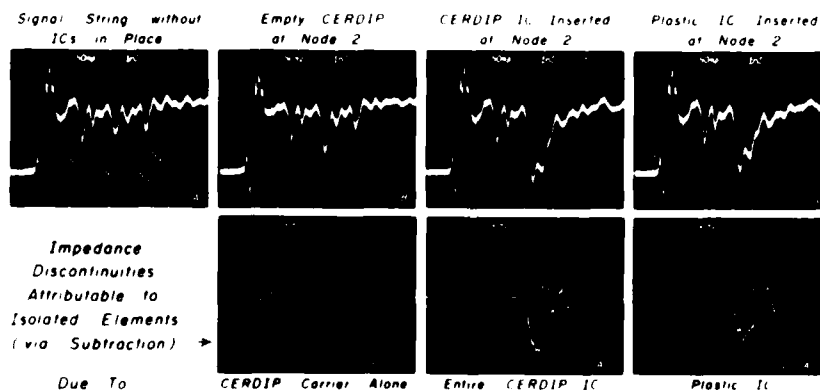


Figure 31

no integrated circuits installed; the second from leftmost figure in the upper row depicts the impedance discontinuity caused by an empty Cerdip inserted at node 2. The leftmost panel in the lower row shows the impedance discontinuity caused by the Cerdip carrier alone (panel B minus panel A). In panel C, a completely functional Cerdip with encapsulated subnanosecond ECL dice was inserted at node 2, and in panel D a subnanosecond ECL dice encapsulated in a plastic package was inserted at node 2. Panel (C-A) and panel (D-A) depict the impedance discontinuity due to the entire Cerdip IC (panel C minus panel A), and the impedance discontinuity caused by a

**EFFECTS OF INTEGRATED CIRCUIT AND PACKAGE INPUT CAPACITANCES  
UPON IMPEDANCE OF MULTI-NODE SIGNAL STRING**

(Measurements by Time Domain Reflectometry;  
Subnanosecond ECL ICs in Plastic and Cerdip Packages;  
Interconnects via 75  $\Omega$  Wire-Wrappable Coax; Package End Pins Tested Only)

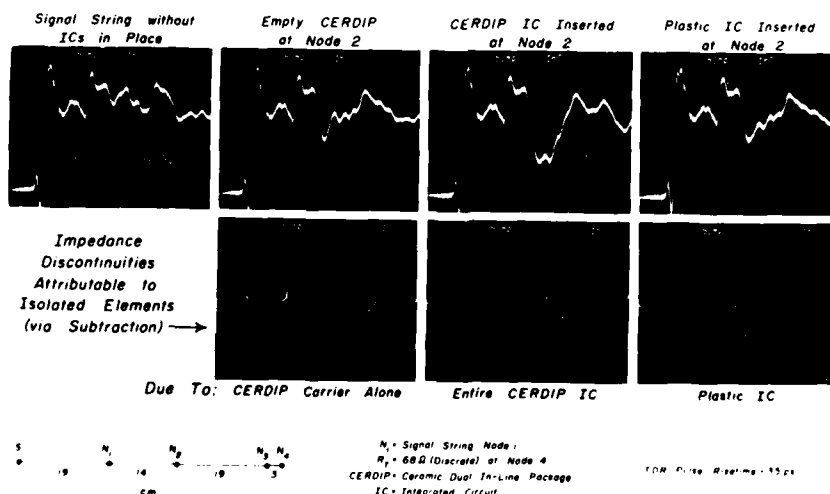


Figure 32

plastic-encapsulated subnanosecond ECL dice (panel D minus panel A). Note that the empty Cerdip carrier contributes an impedance discontinuity, which becomes even larger for the complete Cerdip-encapsulated dice. The plastic encapsulated dice shows a considerably smaller impedance discontinuity than does the Cerdip package, for both the center and end pins, although the difference is more pronounced for the end pins than for center pins. The small two-digit numbers which appear just above the discontinuities in the lower row of panels are the area of the discontinuity in units of millirho-nsec; the best measure of the disruptive effect of such a discontinuity on signal string performance is neither the amplitude nor the duration of the discontinuity, but the product of these values. As will be described in a later section, the findings of these TDR studies were corroborated by the performance of the operational circuits; that is, for equivalent signal strings, the duration and magnitude of voltage reflections is lower, and signal rise/fall times are faster, when the plastic encapsulated dual in-line packages are substituted for the Cerdips.

#### TDR Comparison Tests of ECL Dice Encapsulated in Ceramic Dual In-Line Packages and Ceramic Leadless Chip Carriers

Although TDR studies indicate that plastic encapsulation improves the reflection characteristics of the integrated circuits, it is reasonable to expect additional improvements by employing an encapsulation of smaller physical size, smaller

amounts of bonding and padout metal, and closer physical spacing between the silicon dice and the outer boundary of the package. In order to test this hypothesis, we arranged to have 100 sub-nanosecond ECL devices of two generic device types packaged in small, ceramic leadless chip carriers (3M Corporation Part #ST-88-524-AC). Figure 33 depicts time domain reflectometry measurements from a test jig fabricated with these components. Subtraction techniques were used to isolate the impedance discontinuities caused by the integrated circuit, dice and bond wires and by the leadless chip carrier. Comparison of the results of Figures 31 through 33 indicates that the integrated

**EFFECTS OF INTEGRATED CIRCUIT,  
PACKAGE, AND PROBE INPUT CAPACITANCES UPON IMPEDANCE  
OF MULTI-NODE SIGNAL STRING**  
(Measurements by Time Domain Reflectometry; Subnanosecond ECL Components in  
3M Ceramic Leadless Chip Carriers; Interconnects via 70Ω Semirigid Coax)

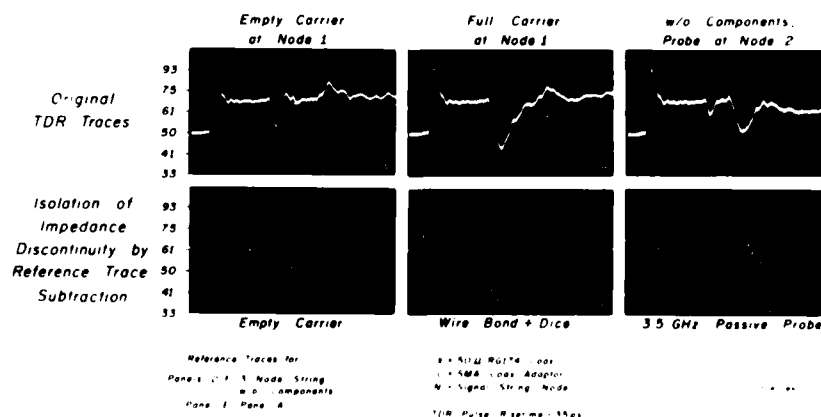


Figure 33

circuit encapsulated in a ceramic chip carrier causes 25-50% less line disturbance than does the Cerdip-encapsulated dice when center and end pins are tested, but creates 15-50% greater disturbance than does the plastic-encapsulated integrated circuit when center and end pins are tested. These comparison results between ceramic chip carrier and plastic DIP encapsulation were unexpectedly in favor of the plastic DIP rather than of the ceramic leadless chip carrier (further operational tests will be presented in the following sections).

#### Operational Comparison Tests of Plastic DIP-Encapsulated and Ceramic DIP-Encapsulated ECL Dice

Figures 34 through 36 demonstrate the operational performance differences between systems containing ECL dice encapsulated in ceramic and in plastic packages resulting from the lower input shunt capacitances of the plastic package. These figures depict the results from test strings consisting of a driver gate, three destination nodes, and a terminator pack resistor. The separation between consecutive circuit nodes is diagrammed at the bottom of each figure; 70 ohm semirigid coax was employed for all interconnects. For one set of experiments, the test strings were established with end pins of the dual in-line packages (Figures 34 and 36), while for the second experiment only center pins were included in the string (Figure 35). The source gate was driven at a 50 MHz clock rate (Figures 34 and 35) and at a 125 MHz rate (Figure 36).

EFFECTS OF ENCAPSULATION MATERIAL  
ON ECL INTEGRATED CIRCUIT ELECTRICAL CHARACTERISTICS  
AT HIGH CLOCK RATES  
(50 MHz System Clock; Signal String Composed of End Pins Only,  
Interconnects via 70  $\Omega$  Semirigid Coax)

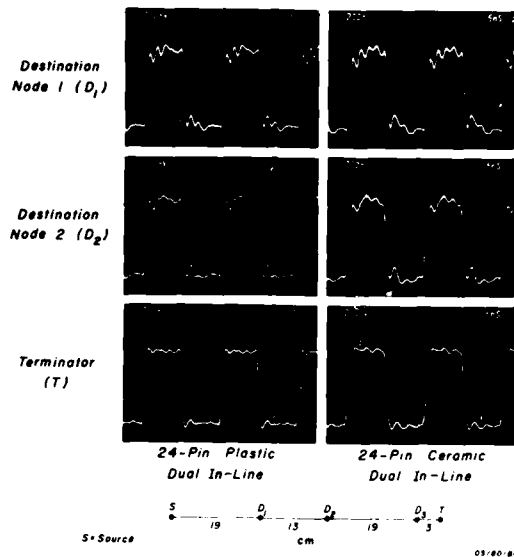


Figure 34

Two cases were examined: In one case, the components inserted into the signal string were encapsulated in standard 24-pin Cerdip packages (rightmost column of panels in each figure); in the other case, plastic encapsulated DIP's with integral heat sinks were employed. For each operating frequency, component type, and pinout combination being studied, the operating signal strings were test-pointed at the first

EFFECTS OF ENCAPSULATION MATERIAL  
ON ECL INTEGRATED CIRCUIT ELECTRICAL CHARACTERISTICS  
AT HIGH CLOCK RATES  
(50 MHz System Clock; Signal String Composed of Center Pins Only;  
Interconnects via 70  $\Omega$  Semirigid Coax)

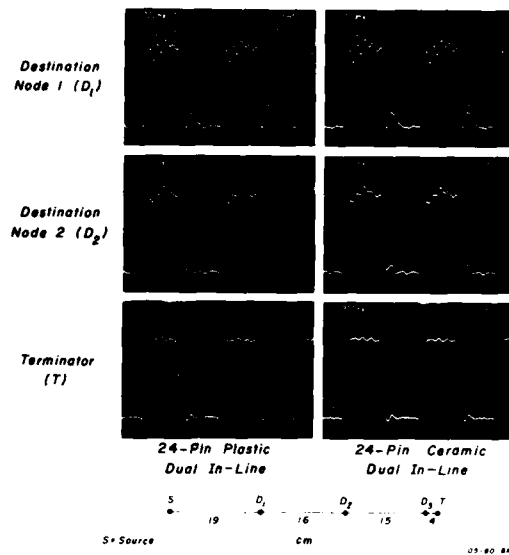


Figure 35

and second destinations in the string, and at the string terminator resistor. In all panels of Figures 34 and 35, the small sinusoidal disturbances observed on the waveforms just following the rising and falling edges of each rectangular pulse are caused by reflections traveling back and forth on the lines which originate from the input capacitances of each destination node. For example, the wavefronts in the uppermost

EFFECTS OF ENCAPSULATION MATERIAL  
ON ECL INTEGRATED CIRCUIT ELECTRICAL CHARACTERISTICS  
AT HIGH CLOCK RATES  
(125 MHz System Clock; Signal String Composed of End Pins Only;  
Interconnects via 70  $\Omega$  Semirigid Coax)

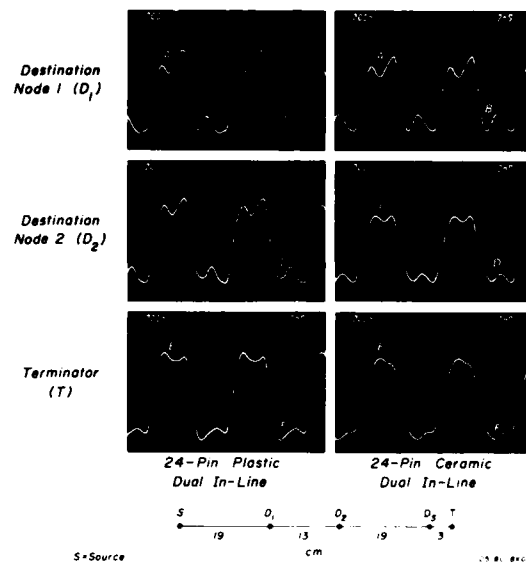


Figure 36

row of images of Figure 34, recorded from the first destination node ( $D_1$ ) position, show two major negative disturbances at letter "A" corresponding to the reflections from the circuit pins at nodes  $D_2$  and  $D_3$ ; just following the falling edges of these traces negative reflections can also be observed at letter "B"; again two small peaks are identified, corresponding



to the reflections caused from nodes D2 and D3. Similarly, the middle row of figures depicts measurements recorded from the D2 position; in both middle panels, only single reflection peaks are observed at letters "C" and "D" respectively, corresponding to those generated by reflections from the D3 node. The lower row of panels shows similar measurements recorded from both test signal strings at the location of the terminator; these waveshapes appear the least disturbed of all at letters "E" and "F" since the terminator receives only the initial wavefront (either rising or falling) and should not itself create any reflections. The small amounts of nonuniformity at the tops and bottoms of the waveforms recorded at the terminator are caused by 1) third level reflections, which have traversed the transmission line through  $1\frac{1}{2}$  one-way passages of the line, that is, from the source to the destination nodes D1 through D3, back to the source, and then again back toward the terminator; 2) by small amounts of noise introduced through the - 2 V supply bus (but not through terminator pack cross-talk, since only the test string was terminated on the pack); and 3) by small amounts of transmission line propagation non-uniformities (i.e., "modeing").

The results of these three experiments may be summarized as follows. Due to the lower input shunt capacitance of the plastic DIPs, the rise/fall times of their associated signals are more rapid, and the pulses have a squarer conformation than do those of the Cerdip devices. This phenomenon can be

readily observed in Figure 36 by comparing the left and right panels in each row. Reflection amplitudes are slightly less for the plastic components than for the ceramic, but not sufficiently less to improve signal conformation markedly. Finally, there is an operational difference between end and center pins on the dual in-line packages of both types; comparison of Figures 34 and 35 indicates that the magnitude of reflections from center pins is slightly less than from corner pins, since the internal lead frame foils are longer (and hence exhibit larger series inductance and shunt capacitance) for the end pins. The plastic encapsulation clearly does result in improved signal string performance by minimizing shunt capacitance across the transmission line. However, it is also apparent from these experiments that the reflections caused by the dual in-line package systems are always present regardless of whether plastic or ceramic substrate encapsulation is employed.

#### 1 GHz Operation of Special ECL Components Fabricated With Wire Wrap Protocol

As a verification that the logic panel and wire wrap interconnect protocol described in prior sections of this report were not responsible for the signal string secondary reflections, advanced ECL components fabricated by Fairchild Camera and Instrument Corporation with their new Isoplanar S integrated circuit technology (transistor  $f_T$  values are approximately 6.5 GHz)

were obtained in specially designed miniature dual in-line packages. These special components were installed on the ECL logic panel of Figure 11 and driven by a clock signal from a commercial clock generator. The signals were led into the board on RG 174 50-ohm coaxial cable, then through 6 inches of single-rail twisted pair wire, and terminated on the input to the circuit (a divide-by-four prescaler) with a discrete terminator resistor. The output from the prescaler was terminated on a pack resistor through 6 inches of twisted pair wire. The source clock rate was gradually increased to approximately 1 GHz. The lower trace of Figure 37 shows the clock signal, which appears sinusoidal because of the low-pass frequency characteristics (oscilloscope amplitude response is -3 dB at 1 GHz) of the Tektronix 7104 oscilloscope. The upper trace shows the divide-by-four

*HIGH FREQUENCY PERFORMANCE OF ADVANCED-DESIGN  
SUBNANOSECOND EMITTER COUPLED LOGIC (ECL) COMPONENT  
AND WIRE WRAP INTERCONNECT TECHNOLOGY*

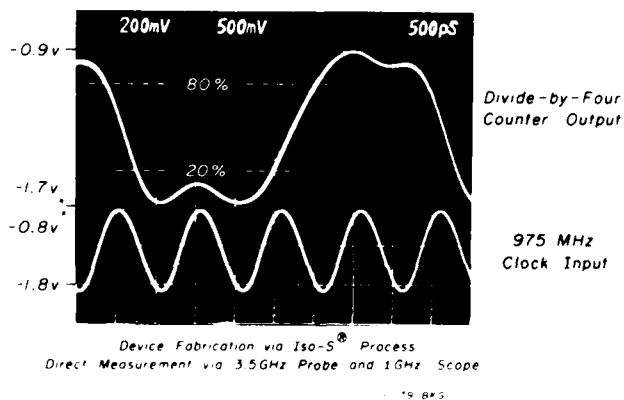


Figure 37

output of the high speed counter, which operated with no missed transitions. These results indicate that the board and interconnect technology are capable of supporting clock rates well in excess of the 250 MHz maximum rate observed in the test circuits of Figures 27 and 28.

Based upon a number of these measurements, it is now apparent that the major cause of reflections in the dual in-line package configuration cannot be alleviated merely by the choice of encapsulation material; the physical size, dimensions, and lead frame layout required in the 24-pin dual in-line package configurations are too large to permit optimum performance of the ECL dice. It is also now apparent (as a result of the multiple studies described in this report) that the major impediment to achievement of maximum performance from the subnanosecond ECL dice is not the wire wrap protocol, the type of logic panel described herein, interwire crosstalk, terminator induced crosstalk, or power plane noise, but from the reflections caused by the dual in-line packages. The only way to improve performance of these circuits up to their vendor-guaranteed levels will be through the adoption of new packaging with lower input shunt capacitance and shorter contact runs within the package.

#### Possible Circuit Performance Improvements Obtained by Conversion to Leadless Chip Carrier Encapsulation

To investigate the possibility that the subnanosecond ECL

dice packaged in leadless chip carriers would demonstrate improved electrical performance, we arranged to have 100 ECL dice of two generic part types packaged in 24-pin ceramic leadless chip carriers (3M Corporation Part #ST-88-524-AC, indicated by "LC4" in Figure 38). The ceramic leadless chip carrier dimensions are 0.045 inches thick, 0.4 inches square. The six pad contacts on each edge of the chip carrier are separated by 0.050 inches. The small size of these devices in comparison to the CerdIPs is apparent in Figure 38. A small two layer copper-clad brassboard test circuit was fabricated

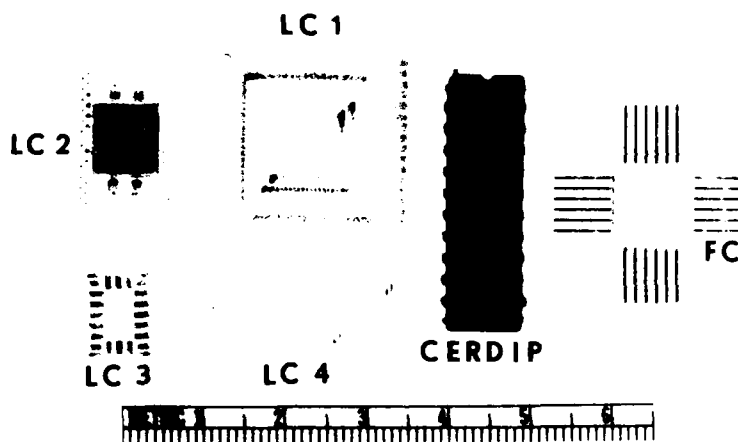


Figure 38

VARIOUS PACKAGES IN USE OR UNDER CONSIDERATION  
FOR SUBNANOSECOND ECL. FC = CERAMIC FLAT PACK  
CERDIP = 24-PIN CERAMIC DUAL IN-LINE PACKAGE; LC1-LC4:  
FOUR STYLES OF CERAMIC LEADLESS CHIP CARRIER.

with lead tab contact spacing to match the padout spacing of the leadless chip carriers; twisted pair interconnects were then bump soldered to the copper clad printed circuit card (Figure 39); the logical design of the circuit installed on the brassboard was identical to that of Figure 27.

A series of time domain reflectometry and operational tests were then undertaken. The upper left panel of Figure 30

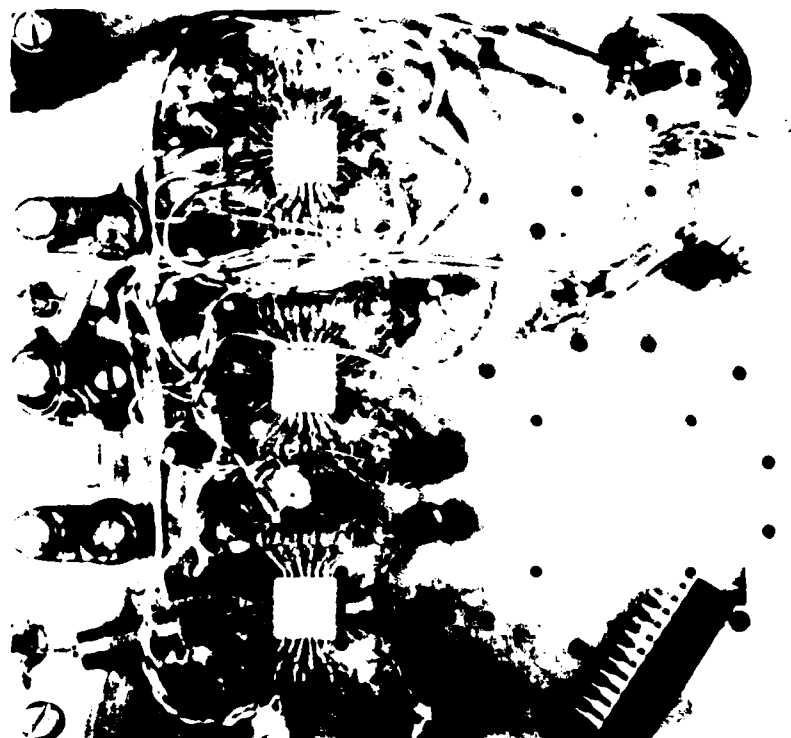


Figure 39

SMALL PROTOTYPE BRASSBOARD TO TEST PERFORMANCE OF THE  
DEVICES PACKAGED IN CERAMIC LEADLESS CHIP CARRIERS  
(LABELED 100102 and 100151). SCALE OF PHOTOGRAPH IS 1:1.

depicts the time domain reflectometry trace measured with the three-node transmission line in place and with an empty ceramic chip carrier bump soldered onto the brassboard at node 1. The middle panel, upper row, shows the significant impedance discontinuity caused by bump soldering a fully loaded ceramic chip carrier onto the brassboard at node 1. The upper right panel demonstrates that the placement of a 500 ohm, 3.5 GHz passive test probe at node 2 creates a large impedance discontinuity as well. As described earlier, subtraction techniques were then employed to isolate the impedance discontinuities caused by the separate components of the ECL dice in its chip carrier encapsulation. The area under the impedance discontinuity caused by the leadless chip carrier is substantially smaller (13 millirho-nsec) than that caused by an empty ceramic dual in-line package, as observed in the lower left panel of Figure 32 (76 millirho-nsec). The middle panel in the lower row of Figure 33 depicts the parasitic capacitance caused by the wire bond and ECL dice. The total impedance discontinuity area for the chip and its chip carrier is less (101 millirho-nsec) than that for an identical ECL chip packaged in a CERDIP (153 millirho-nsec in Figure 32).

The leadless chip carrier brassboard was then tested operationally to ascertain whether the maximum achievable clock rate would exceed the 250 MHz maximum usable frequency observed for the ECL dice in CERDIP packages. Figure 40 displays results from these studies. The circuit was able to

PERFORMANCE CHARACTERISTICS OF PROTOTYPE  
SYNCHRONOUS SUBNANOSECOND ECL CIRCUIT  
EMPLOYING LEADLESS CHIP CARRIER ENCAPSULATION  
(454 MHz System Clock via Square Wave Oscillator,  
Carriers Bump Soldered to PC Board)

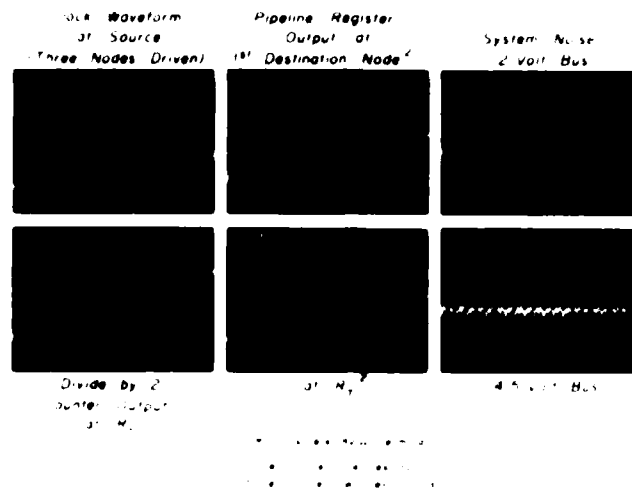


Figure 40

operate correctly up to a clock rate of 454 MHz, the highest usable clock rate for any subnanosecond ECL circuit which we have achieved to date. The system noise on the -2 V bus and -4.5 V bus is of greater magnitude than that of the integrated circuits packaged in CERDIP. However, the small test circuit of Figure 39 was fabricated on a crude brassboard without adequate power plane decoupling, and, displayed noise characteristics reminiscent of the early dual in-line package brassboard studies (Figures 1, 2, and 5). The waveforms depicted in the four leftmost panels of Figure 40, while retaining a small



amount of residual reflection effects, are nonetheless considerably "cleaner" than those from test circuits fabricated with Cerdips. These studies confirm that maximum performance of the ECL dice can probably be achieved only by eventual conversion to leadless chip carriers.

## SECTION 6

### INVESTIGATION OF INTERCONNECT PROTOCOLS FOR HIGH SPEED CLOCK AND DATA SIGNALS BETWEEN MULTIPLE LOGIC PANELS

#### Protocols for Introduction of High Speed Clock Signals Into Logic Panels in a Multiboard System

In a very large multiboard digital system fabricated with subnanosecond ECL and operating at high clock rates or with multiphase clock signals, all boards must receive clock signal feeds with identical and stable phase relationships. Although the clock signal may be introduced via the logic panel edge connectors along with the data signals (see the following discussion of multiconductor cables), it is also possible to inject the clock waveform into the geometric center of each logic panel from a common drive source using single ended or differential drive on miniature coaxial cables. This approach is attractive because of the low dispersion loss, high inherent shielding, and high impedance stability which is characteristic of the RG 17X series miniature coax.

The clock feed protocol tested here employs 50 ohm RG 174 coax, SMA cable connectors, and a small SMA connector carrier (Augat, Inc., Part #101 HG1) configured for direct insertion into any integrated circuit socket on the logic panel. This clock feed mechanism is apparent in Figure 10, including the

RG 174 coaxial cable and SMA cable connector, and the header containing two SMA connectors. The double header structure allows the injection at a single location of a two-phase clock signal (with each phase transmitted via a single ended protocol), or of a single phase clock signal transmitted using a "dual single-ended" protocol, described below, via two coax cables. Figure 41 depicts the results of time domain reflectometry measurements made on a single-ended, single phase clock injection protocol using the RG 174 coax, SMA cable connectors, and SMA header. The uppermost trace shows the impedance discontinuity, labeled BS, resulting from a BNC/SMA cable coupling which converts the TDR output cable (a 50 ohm semirigid coax) to the RG 174 coax. The letter C delineates the impedance discontinuity created by the SMA cable connector and SMA header plugged into the circuit board. The signal wavefront propagates through the RG 174 cable and SMA cable connector into the header, and into the twisted pair Kynar wire which leads the signal to the distribution driver gates on the logic panel. The vertical scale on the upper trace is 100 millirho/cm; the lower trace depicts the same measurement but at a vertical scale sensitivity of 50 millirho/cm. The impedance discontinuity between the 50 ohm coax and the 75 ohm twisted pair backplane wiring can be clearly seen. Note that the percent impedance discontinuity caused by the SMA cable connector and SMA header structure is 20%, resulting in an approximately 10% voltage reflection, while the percent impedance discontinuity of a BNC/SMA coupling specially designed for this type of application is 22%.

**PERFORMANCE COMPARISON VIA TIME  
DOMAIN REFLECTOMETRY OF TWO  
TRANSMISSION LINE COUPLINGS FOR  
USE WITH SHORT RISETIME  
SINGLE-ENDED DIGITAL SIGNALS**

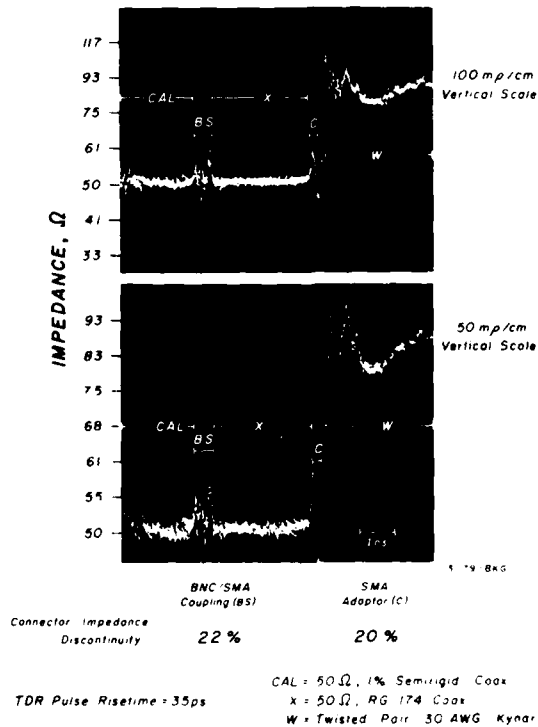


Figure 41

The single-ended version of this clock feed structure has been successfully employed to supply the clock waveforms for the test circuits of Figures 28, 29, and 37, whose data represents system clock rates of 250 MHz, 350 MHz, and nearly 1 GHz respectively. This clock feed protocol has also been incorporated into all three of the Engineering Demonstration Test Circuits fabricated for this project (described in Section 8 of this report) and appears stable and repeatable. For

multiboard systems required to operate in very noisy environments, an even more secure clock feed structure can be established by using a pair of RG 174 coax feeds, with the clock signal driven in a so-called "dual single-ended" mode. In this specialized clock feed protocol, first introduced in Section 3 of this report, the true and complement outputs of the driving gate are each fed to the center conductors of two coax cables, whose shields are grounded at both ends. At the receiver end, the two center conductors are each connected to the true and complement input pins on the differential line receiver and then each terminated through separate 50 ohm resistors (assuming 50 ohm coax) to -2 V. The true and complement sides of the clock signal are thus each transmitted on single ended coax, but received differentially. Figure 52 depicts operational measurements of a clock drive using this protocol.

Stable transmission of dual single-ended clock signals up to 368 MHz has been achieved with this system over cable lengths of 250 cm using an ECL gate as the source driver; the shielding of the center conductors makes this protocol highly immune to external interferences in a noisy environment. The protocol is thus well suited to transmission of ECL gate-driven clock signals to multiple logic panels in a large ECL processor system, though it is an impractically expensive protocol for transmission of word-wide data between logic panels. Additional comments regarding this protocol are presented later in the discussion of interboard clock and data transmission.

## On-Board Clock Distribution Via Fanout Through Single Level and Dual Level Trees

Tightly controlled protocols for fanout of the clock signal on each logic board are mandatory for subnanosecond ECL systems designed to operate at high clock rates, particularly when several logic panels are linked together in a large processor system. Layout of clock strings is one of the most critical portions of the design of a high speed ECL system. Because clock signals are more sensitive than data signals to the wavefront degradation caused by reflections from destination nodes (see the discussion of this problem in prior sections), the number of integrated circuits which are driven from a single ECL clock drive gate must be severely restricted. Based upon the fabrication of a half dozen operational systems to date, for clock frequencies up to approximately 50 MHz, no clock string is permitted more than six to eight destination nodes (not including the terminator); at clock rates above 100 MHz no clock string can contain more than three to four destination nodes. A logic board containing 200 integrated circuits would thus require from 35 to 65 separate clock strings, under the worst case assumption that all circuits on the board are clock-driven part types. Such large numbers of clock strings cannot be driven by a single integrated circuit, since even a specialized clock driver component such as the F100112 can drive only eight "true" and eight "complement" clock strings.

When the number of clock strings required on a single logic board is less than the drive capacity of a single clock drive chip such as the F100112, a single level clock fanout is used. The clock signal entering the board through a coax cable and SMA header in the center of the board should be immediately terminated with the shortest possible wire at the common input pin of the clock drive chip (e.g., on pin 19 of the F100112 clock drive chip packaged in Cerdip). Layout of clock strings from the clock drive chip should be carried out such that 1) all integrated circuits driven by a single clock string are as closely spaced on the logic board as possible, preferably within a diameter of 1.5-2.0 inches; and 2) the lead wires from the driving gate to the first destination for all clock strings on the board should be cut to the same length. If this protocol is adhered to from the onset of design, problems of slivers and runt pulses encountered during final system checkout will be minimized.

When the number of clock strings on a single logic board exceeds the drive capacity of a single clock drive chip, a two-level clock fanout protocol should be employed. In this case the outputs from the "first level" clock drive chip are used to drive the common driver inputs of several "second level" clock driver chips positioned uniformly around the logic board; it is the outputs from these second level clock driver chips which are in turn used to drive the working circuits on the board. At this point several warnings are necessary if a

two level clock fanout structure is to be employed. 1) The first level clock driver chip should be used only to drive second-level clock driver chips, but never other integrated circuits on the logic board. 2) All wires between the first level clock drive chip and second level drive chips should be cut to the same length. 3) All wires between second level drive chips and the first destination node of each second level clock string should be cut to the same length. 4) The risetime and faltime of ECL gates are usually not identical, because the active gate pulls the logic level HIGH, but the logic string terminator resistor pulls the logic level LOW; in addition, the output impedance of the drive gate and the terminator resistor are quite dissimilar (7 ohms and 50-100 ohms respectively). Hence, a chain of gates driving one another, in which a square wave clock signal feeds the input of the first gate, and the true output of that gate feeds the second gate, and so on, can occasionally result in the clock output from the  $N^{\text{th}}$  gate being no longer square (i.e., the duration of the logic HIGH portion of the waveform is no longer the same as the duration of the logic LOW). Such loss of clock waveform symmetry can be a very serious problem if both half-cycles of the clock waveform are employed for the execution of logical subtasks, since one half cycle will be longer than required and the other half cycle will be less than required. This loss of symmetry of the clock signal in a two-level clock fanout can be avoided by using the complement outputs of the first level clock chip to drive the inputs of the second-level clock chips,



and then using the complement outputs of the second-level clock drive chips to drive the other integrated circuits on the board.

5) In extremely noisy environments requiring absolute stability and security of the clock signals, the second level clock driver chips are replaced by differential line receiver components such as the F100114. The first-level clock driver then transmits a differential clock signal to each of the second-level clock drivers, which receive the clock signal differentially and retransmit in single-ended mode to the other clocked components on the logic board.

Experience with a half dozen subnanosecond ECL systems fabricated to date in this laboratory indicates that design and packaging decisions intended to minimize composite noise and crosstalk should be made on the basis of the "composite clock frequency" at which the system will be operated. The composite clock frequency is defined here as the product of the basic clock rate and the number of phases employed. For example, a four-phase 40 MHz clock is in effect a "composite clock frequency" of 160 MHz, referred to in this laboratory as the "clock edge rate". Since all forms of noise and crosstalk occur only when logic states are changed, i.e., at the (positive) transitions of all phase clocks, system disturbances will occur at the edge rate, not at the clock rate. If complements of the positive clock phases are also employed in a design, the clock edge rate must be increased to account for these "negative" clock phases as well. Since many of the

edge-related disturbances exhibit decay times of 2-10 nsec, their effects can overlap temporally and add algebraically. Hence, a 40 MHz four-phase clocked system should be designed with the precautions normally reserved for a much higher frequency 160 MHz single-phase system if maximum stability is to be assured.

#### Investigation of Protocols for Interboard Cabling for Bus Oriented Transmission of Data Signals

Several feasible protocols have been identified for very high speed data communications pathways between multiple logic panels in a large prototype system, including unidirectional differential transmission, and unidirectional single-ended transmission with at least one ground lead for each signal. Single conductor transmission, which exhibits extremely poor crosstalk immunity at high system clock rates, has proven totally unreliable in our studies and will not be discussed further in this report. Although the use of mass terminatable multiple coaxial cables would be expected to yield minimum signal crosstalk, we have been able to demonstrate that differential transmission via high quality woven twisted pair cable regains all of this crosstalk immunity, is less susceptible to reflections and standing waves, and is considerably less expensive to implement. Although we have designed and installed party line or daisy chain interboard protocols in specialized systems, they are strongly discouraged since they

possess considerably poorer noise immunity (Reference 3) than dedicated unidirectional protocols employing a single transmitter and a single receiver for each transmission line. A bidirectional protocol has been suggested, which is based upon a specialized bus transceiver component not yet available from the first-source component vendor (Reference 3) and only recently announced by an alternate vendor; operational testing of this approach will be required to verify noise immunity characteristics at high operating frequencies.

#### Interboard Cabling Protocol Testing Via Time Domain Reflectometry

High interboard transmission bandwidth can be preserved by matching the impedance of the board wiring, the cable/board connector assemblies, and the signal cable to minimize wavefront reflections at the board/cable interfaces. Figure 42 depicts the results of TDR studies of two methods for establishing logic panel-to-cable interconnects. In the leftmost column a wire type (30 AWG Kynar-coated twisted pair) was selected with a characteristic impedance considerably different from that of the interboard cable material. The resultant substantial impedance discontinuity at the cable connector causes significant wavefront reflections which travel back and forth on the cable, degrading signal risetime and the ability of the line receivers to detect threshold crossing times with high pulse-to-pulse stability. In the rightmost panels, a wire type (30 AWG Teflon-coated twisted pair) was selected with a

TIME DOMAIN REFLECTOMETRY CHARACTERIZATION  
OF TRANSMISSION LINE INTERCONNECTION METHODS  
FOR SHORT RISETIME DIFFERENTIAL DIGITAL SIGNALS

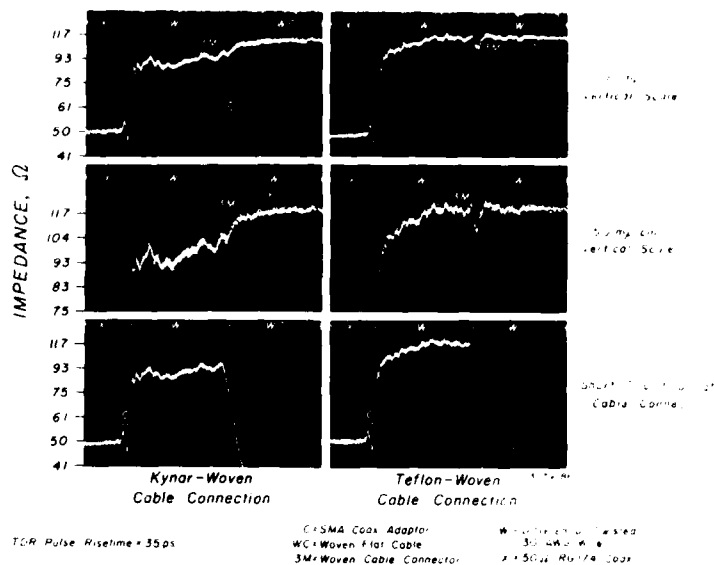


Figure 42

characteristic impedance as close as possible to that of the woven cable, thus confining the impedance discontinuity to the connector itself. Appropriate selection of the connector type results in an impedance discontinuity of both minimum magnitude and minimum duration (in this example, approximately ten percent in impedance magnitude and 400 ps in duration). Corresponding worst case voltage reflections are five percent in amplitude, 400 psec in duration, and negative (i.e., in the direction of the threshold voltage). Alternately, as an extrapolation of the results of Figure 42, slightly lower impedance cable and board wiring material could have been identified which

more closely match the impedance of the connector, thereby completely smoothing out the connector impedance discontinuity.

Figure 43 depicts the results of TDR measurements of four types of cable potentially suitable for interboard signal cabling. The 75 ohm multicoaxial ribbon cable (Amp Corporation 1-226-807-0), and the 93 ohm multicoaxial ribbon cable (Amp Corporation 1-226-812-0), both of which can be mass terminated, are the most costly per unit length per signal, and also display the best impedance uniformity over their entire length (all four cables were cut to 250 cm lengths for this test). However, the impedance nonuniformities of the flat ribbon (3M Scotchflex 3365/26, 13 pair) and woven twisted (Woven Electronics T-13TP2807UL1568N, 13 pair) cables are not large enough to pose significant reflection problems. The impedance characteristics of these cable types vary with the manner in which they are driven. The woven twisted cable impedance is 86 ohms in the single-ended, twisted-with-ground mode, and 110 ohms when driven differentially. The impedance of the flat ribbon cable is 150 ohms in the single-ended-with-ground mode, and in the range of 140-190 ohms in differential mode. Impedance discontinuities at the cable connector/twisted pair wire interface are largest for the flat ribbon cable, and smallest for the 93 ohm multicoax in this test, although these discontinuities could have been reduced by more careful selection of twisted pair wire material and cable connector design to match the impedance of the interboard cable employed (e.g.,

IMPEDANCE CHARACTERISTICS OF VARIOUS  
 INTRABOARD CABLING PROTOCOLS FOR SUBNANOSECOND E. L. SYSTEMS

(All Measurements via Time Domain Reflectometry,  
 Assuming Single Ended Drive)

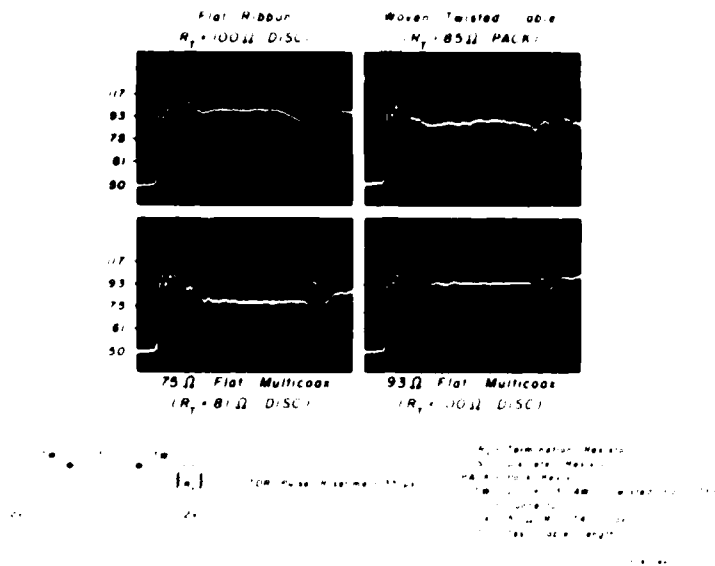


Figure 43

in this study, a smaller impedance discontinuity could have been achieved by replacing the twisted pair Teflon-coated wire with twisted pair Kynar for the flat ribbon cable and 75 ohm multicoax TDR tests). The four cable types tested in Figure 43 do not allow completely interchangeable usage; although the flat ribbon and woven twisted cables can easily accommodate either single-ended or differential transmission protocols, the multicoax cable can only accommodate single-ended protocols which, as will be demonstrated below, are less immune to noise and crosstalk. Although a pair of coax cables in the ribbon multicoax could be used in the dual single-ended mode described

earlier, this is an extremely expensive approach which can be justified only for high frequency clock signals which must remain free of contamination in high noise environments.

#### Verification of Various Interboard Interconnect Protocols Via Operational Testing

The ability of interboard cabling to support high clock rate word-wide transmission of data between logic panels in a subnanosecond ECL environment is bounded at the upper end of the frequency range by various parasitic noise and cross-talk phenomena, the magnitudes of which will vary with the type of transmission protocol used and with the physical characteristics of the cables. The various contamination phenomena can be divided into several categories, including those caused by 1) the appearance of standing waves on the transmission lines; 2) the occurrence of high frequency reflections which do not achieve standing wave status; 3) the introduction of noise into each transmission line by electrostatic and electromagnetic crosstalk from adjacent transmission lines in the same cable; and 4) the introduction of common-mode noise introduced into both wires of the transmission line pair from sources outside the cable. To quantify the magnitudes of these effects individually, appropriate test jigs were established; the results of these tests are described below.

## Susceptibility of Interboard Cabling Protocols to Crosstalk-Induced Electrical Noise

Tests were made of the susceptibility of transmission lines in various types of multiconductor interboard cabling to crosstalk from other transmission lines in the same cable. Four different cable materials were tested, including flat ribbon cable, woven twisted pair cable, as well as 75 ohm and 93 ohm flat multicoax ribbon cable; the multicoax cables were tested only in 250 cm lengths, but the flat ribbon and woven twisted pair cables were tested in 25 cm, 100 cm, and 250 cm lengths. Tests were carried out with single-ended paired-with-ground transmission protocols and also with differential transmission protocols for the flat ribbon and woven twisted pair cables; the 75 ohm and 93 ohm multiple coax cables were studied only in the single-ended transmission mode. To establish the test jig, a pair of high speed F100136 4-bit counters were positioned on a large ECL logic panel and clocked with a high speed commercial clock generator. One of the counters was operated as an up-counter, while the other counter was operated as a down-counter; both counters were allowed to free-run without an initial master reset. The output drives from these counters were then fed in random order to the cable connectors on the logic panel. The logic panel connections were compatible with the cable connectors for all four cable types, allowing direct plug-in of all of the test cables into the same test jig. Each cable was then plugged into a second, completely



separate logic panel of the same type, where a number of ECL line receivers received the transmitted signals. When differential protocols were being measured, the ECL line receivers were wired in the differential mode; when single-ended protocols were being tested, the line receivers were rewired for single-ended reception.

All noise measurements were made at the input pins of the line receivers, between local board ground at the receiver chips and one of the signal lines. In the case of the flat ribbon and woven twisted pair cables, the grounded wire of the pair was chosen at random, while for the multicore, the noise voltage on the center conductor was measured. For these crosstalk studies, a single transmission line pair in the center of the cable was established with a line transmitter and line receiver at the two ends, respectively; however, the input of the line transmitter of the line under test was pulled down to -2 V, as was the terminator resistor at the other end of the line. The transmission line pair on either side of the non-driven string under test was deliberately established as a signal line toggling at the maximum rate, while the wire pair on the other side of the line under test was chosen to be a signal pair toggling at half the maximum rate; this approach insured maximum density of electromagnetic crosstalk with a maximum number of uncorrelated rising and falling edges contributing to the electromagnetic crosstalk fields.

Figures 44 through 47 depict the results of this large set of crosstalk measurements, which may be summarized as follows. For each cable type and transmission protocol, the peak-to-peak crosstalk amplitude increases with increasing cable lengths, though not necessarily in a linear manner (e.g., peak-to-peak noise measured on the flat ribbon cable in the single-ended transmission protocol at the 250 cm length is not ten times the peak-to-peak crosstalk of the same cable and same transmission protocol in the 25 cm length). For all protocols at all cable lengths, the peak-to-peak crosstalk amplitude on the woven twisted pair cable is the same as, or less than, the peak-to-peak crosstalk measured on the flat ribbon cable. In addition, for the flat ribbon and woven twisted cables, the peak-to-peak crosstalk in the differential transmission mode is greater than that in the single-ended transmission mode, regardless of cable type. Lastly, for each cable length, peak-to-peak crosstalk is least for the single-ended paired-with-ground transmission protocol using woven twisted cable; the greatest peak-to-peak crosstalk for each cable length was measured in the differential transmission protocol using two adjacent wires in the flat ribbon cable.

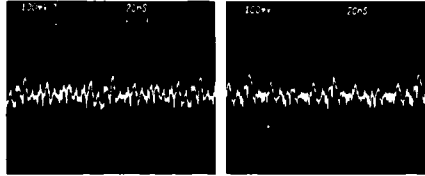
Based upon the comments in the preceding paragraph, it would appear upon first consideration that minimum cable noise could be assured by employing a single-ended paired-with-ground transmission protocol with woven twisted cable, since at the 250 cm length this protocol exhibits a peak-to-peak crosstalk

of 200-250 mV (by comparison, the peak-to-peak crosstalk in the differential transmission protocol for the 250 cm flat ribbon cable is nearly 900 mV). The best protocol is indeed one which uses woven twisted pair cable, since the twisting of the wires tends to cause field cancellation of common mode noise between the two wires of the pair, which cannot be achieved by the side-by-side in-plane conductors of the flat ribbon cable. Since crosstalk is a common-mode type of interference (as can be observed by making differential measurements with a pair of wideband amplifiers and the oscilloscope mainframe in the A - B operational mode), the highest crosstalk immunity is obtained with a differential protocol using the woven twisted wire; differential line receivers such as the F100114 achieve a high rejection capability (Reference 3) for common mode noise signals over a range of +1.5 V to -1.5 V. Although the noise voltages measured from the single-ended protocols in Figures 46, 45, and 44 are less by a factor of two than in the differential case, in the single-ended line receiver configuration all common mode noise rejection capability of the receiver is forfeit. As result, the noise appearing on the input of the line receiver wired in a single-ended configuration contributes directly to a decrease in noise margin of the transmitted signal. In the differential protocol, the noise observed in the lower right panels of Figures 44 through 46 is rejected by the receiver when configured in differential mode. The common mode noise rejection capability of the differential protocol using woven twisted wire is a strong, though not conclusive, argument for this protocol.

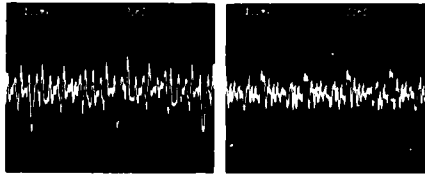
SUSCEPTIBILITY OF VARIOUS SUBNANOSECOND ECL  
INTERBOARD CABLING PROTOCOLS TO CROSSTALK-INDUCED ELECTRICAL NOISE  
(Logic Panels Driven with 100 MHz Clock)

Transmission  
Format

Single-Ended  
Paired with  
Ground



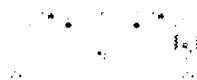
Differential



Flat Ribbon

Woven Twisted

Cable Type (25 cm)



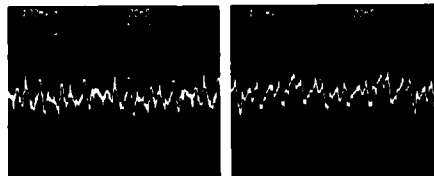
1. Cable connector  
2. Test cable length  
3. 100 cm 1 AWG twisted pair  
4. Single Ended or Differential Protocol  
5. 100 cm 1 AWG twisted pair  
6. 100 cm 1 AWG twisted pair

Figure 44

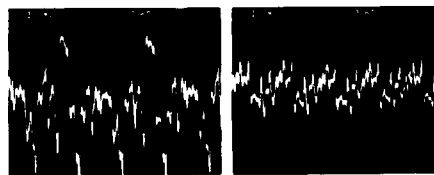
SUSCEPTIBILITY OF VARIOUS SUBNANOSECOND ECL  
INTERBOARD CABLING PROTOCOLS TO CROSSTALK-INDUCED ELECTRICAL NOISE  
(Logic Panels Driven with 100 MHz Clock)

Transmission  
Format

Single-Ended  
Paired with  
Ground



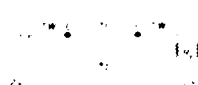
Differential



Flat Ribbon

Woven Twisted

Cable Type (100 cm)



1. Cable connector  
2. Test cable length  
3. 100 cm 1 AWG twisted pair  
4. Single Ended or Differential Protocol  
5. 100 cm 1 AWG twisted pair  
6. 100 cm 1 AWG twisted pair

Figure 45

SUSCEPTIBILITY OF VARIOUS SUBNANOSECOND ECL  
INTERBOARD CABLING PROTOCOLS TO CROSSTALK-INDUCED ELECTRICAL NOISE  
(Logic Panels Driven with 100 MHz Clock)

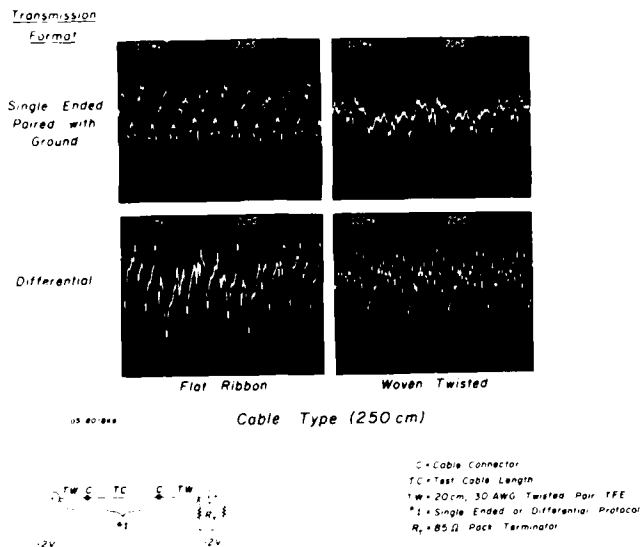


Figure 46

SUSCEPTIBILITY OF VARIOUS SUBNANOSECOND ECL  
INTERBOARD CABLING PROTOCOLS TO CROSSTALK-INDUCED ELECTRICAL NOISE  
(Transmission Format: Single-Ended Paired with Ground;  
Logic Panels Driven with 100 MHz Clock)

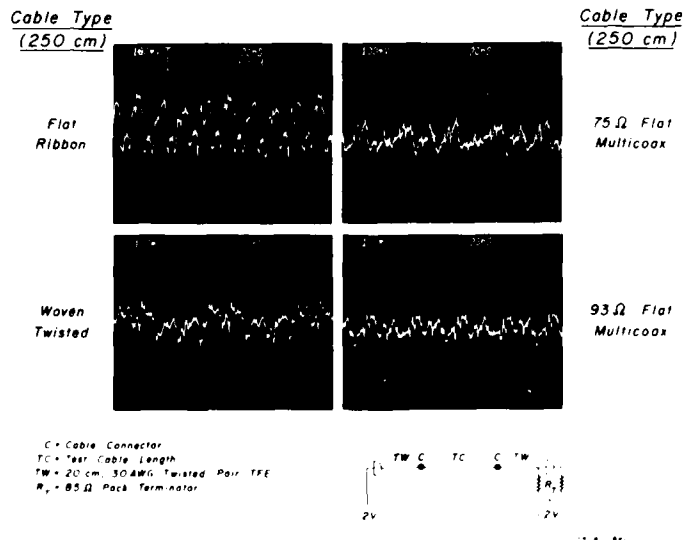


Figure 47

Lastly, the flat ribbon cable, woven twisted cable, and the two styles of multicoax were compared using a single-ended transmission protocol (the only protocol which can realistically be used for the multicoax cables), with all measurements recorded at the 250 cm cable length (Figure 47). The peak-to-peak noise of the multicoax cables is less than that measured for the woven twisted or flat ribbon cables. Peak-to-peak noise in the 93 ohm flat multicoax is marginally less than in the 75 ohm multicoax, probably as a result of differences in cable design and manufacture, which result in more uniform center conductor shielding for the 93 ohm cable. Although the flat multicoax cable can be driven in differential mode between the center conductor and the shield, this is not an optimum drive mechanism for coax because the shield effect is lost (triax cable is usually recommended for such a usage). Similarly, a "dual single-ended" coax drive can be adopted, which is probably the most secure signal drive possible but requires two complete coax cables for each signal. However, multicoax cable is extremely expensive and requires that special mass coax cable connectors be installed at each end of the cable. Since the flat ribbon and woven twisted cables are considerably less expensive, the differential transmission, woven twisted wire protocol has a significant cost/performance advantage over the other protocols.

A note of warning must be given regarding use of the F100114 differential line receiver. The first-source vendor

states (Reference 3, page 10-17): "The F100114 is a Quint Differential Amplifier with emitter-follower outputs. An internal reference supply ( $V_{BB}$ ) is available for single ended reception." The vendor implies without direct statement that if any of the line receivers is to be used in single-ended mode, the  $V_{BB}$  source available directly from the integrated circuit should be connected to the unused input pin of the line receiver gate. However, our measurements indicate that the  $V_{BB}$  current source is not "stiff," but rather undergoes voltage fluctuations exactly in phase with the signal on the true input line of the receiver gate. Hence, the unused complement input is not maintained at a constant reference value but instead also fluctuates with the same conformation and phase as the input signal. Signals identical in phase but slightly different in amplitude on both inputs of the receiver appear to the receiver circuitry to be common mode noise, and tend to be rejected. Hence, the actual transmitted signal can be lost, causing the performance of the F100114 receiver in single-ended mode to be much poorer than that of a standard ECL gate. Resistor or resistor-capacitor decoupling networks connected to the  $V_{BB}$  output have been investigated, with only a slight degree of improvement in  $V_{BB}$  stability noted. Until this problem is resolved by redesign of the integrated circuit, the F100114 should never be employed as a single-ended line receiver; any standard ECL gate will demonstrate better performance in such an application.

## Susceptibility of Interboard Cabling Protocols to Waveform Degradation Via Reflections and Standing Waves

The noise and crosstalk measurements described in the preceding section for multiconductor interboard signal cable present only a part of the performance characteristics of the medium. Degradation of signal cable performance is also caused by reflections and standing waves on each signal line, and by impedance discontinuities at the source, destination, and interboard cable connectors. To test the operational integrity of several types of interboard multiconductor cable, the cable test jig described in the preceding section was modified slightly to allow separate treatment of data bits and clock signals in the same cable (for many bus-oriented cable protocols it is necessary to transmit clock signals along with the data). A conductor pair at the extreme edge of each cable was reserved for transmission of both single-ended and differential clock signals; the pair of wires immediately adjacent to the edge pair were connected to ground at both ends of the cable, thus assuring a one-pair separation and shielding between the clock signal and the next nearest data bit signal. Since the preservation of the clock waveform is of paramount importance, the separation of the clock signal from the data bits in the same cable with the grounded pair is an acceptable usage of one conducting pair, although it would be prohibitively costly to separate each signal bit pair



from its adjacent neighbors in the same manner. Hence, performance differences are apparent for the clock signal and for the data signals. All data bits were routed on adjacent pairs for maximum utilization of the transmission bandwidth of each cable. It must be emphasized that in the tests to be described below, whenever a clock source was required from a commercial clock generator, the clock signal was not employed directly in the test jig, but was always buffered through an F100112 quad line driver. The clock drive tests reported below thus represent clock signal behavior in a totally ECL 100K environment.

As a result of the creation of standing waves and complex reflections in these multiconductor cables, their performance over a range of frequencies from several tens of MHz up to several hundred MHz is both nonuniform and unpredictable. Performance degradation of the cable appears in three modes:

- 1) The pulse-to-pulse duration and conformation of a transmitted square wave signal, that is, the duration between the rising edges of any two consecutive pulses, measured at the output of a bus receiver, gradually becomes quite variable from one pulse pair to the next pulse pair in the same pulse stream and at the same frequency;
- 2) The output LOW-to-HIGH voltage swing decreases from its nominal value of 800 mV toward much smaller values; and
- 3) Short spike-shaped transients gradually appear in the conformation of otherwise square pulse trains.

The criteria used to define the maximum cable performance in

all of the measurements described below were: A degradation in uniformity of interpulse timing measured at the threshold voltage on the rising edges of consecutive pulses, for all pulse pairs, of greater than 10%; a falloff in the peak-to-peak signal swing from 800 mV to 700 mV; and lastly, the appearance of even a single transient spike in any data or clock pulse in an entire pulse train.

A warning regarding interboard cable performance must be presented here. As the test signal being driven through the cable is gradually increased from low to high drive rates, the performance of the cable remains satisfactory at the lower frequencies. The cable output then abruptly degrades; if the test signal frequency is increased still farther, performance improves, and then waxes and wanes through several "cycles" with increasing clock rate. For example, a cable which fails at 100 MHz may appear to perform properly at 175 MHz, then fail at 225 MHz and appear to perform correctly again at 300 MHz. In the following tests, we have rated the performance of each cable as the lowest frequency at which performance degradation was observed. The waxing and waning performance behavior of many types of cable should not seduce the system designer into reliance on the stability of the cable properties above the lowest failure frequency, since cable performance becomes pattern sensitive as signal clock rate is increased above that point.

Optimum Protocols for Interboard Transmission of High Frequency  
Clock Signals Through Multiconductor Cable

Figures 48 and 49 document the ability of woven twisted and flat ribbon cables to transmit high frequency clock signals through an edge pair of conductors over various cable lengths from 25 to 250 cm. The measurements depicted in Figures 48 through 52 were recorded at the output pins of the differential line receivers of the signal lines under test; hence, these measurements characterize the effects of noise and crosstalk on the line receivers as well as on the transmission medium itself. Figure 48 depicts these results when a single-ended paired-with-ground transmission protocol was employed. For a given cable length and a single-ended transmission protocol, the differences in maximum frequency transmission capabilities between the woven twisted and flat ribbon cables are quite significant. For example, at 25 cm lengths, the woven twisted cable faithfully transmits the clock signal to 170 MHz, while the flat ribbon cable is only capable of a 110 MHz maximum rate. Similarly, at the 250 cm cable length, the woven twisted cable driven in single-ended mode is capable of a 90 MHz maximum rate, versus a 50 MHz maximum rate for the flat ribbon cable. Note particularly the small notches in the lower rightmost panel of this figure, representing a spike transient toward the threshold voltage, which in some measurements was observed to cross the threshold voltage and create false inputs to a register following the line receivers. The occurrence of such a

MAXIMUM TRANSMISSION FREQUENCIES OF  
SUBNANOSECOND ECL CLOCK WAVEFORMS DRIVEN  
VIA SINGLE-ENDED PROTOCOLS THROUGH  
MULTICONDUCTOR INTERBOARD SIGNAL CABLES OF VARIOUS TYPES  
(Traces Recorded at Output of Single-Ended Line Receivers)

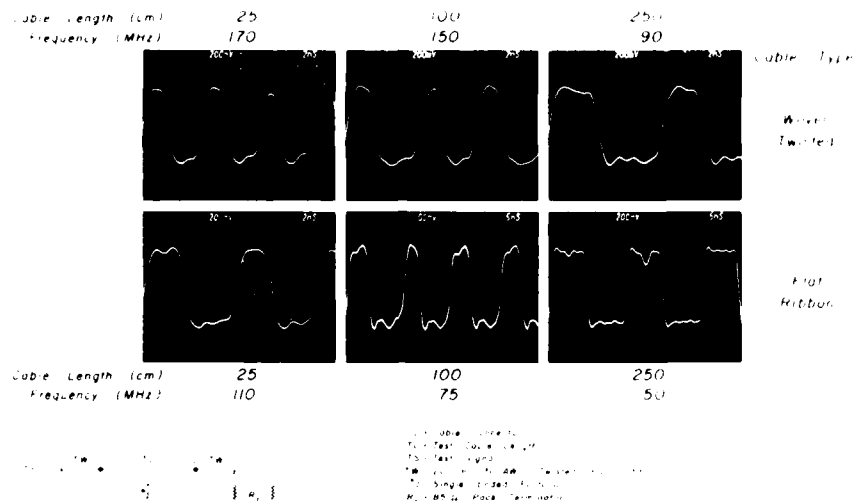


Figure 48

MAXIMUM TRANSMISSION FREQUENCIES OF DIFFERENTIALLY DRIVEN  
SUBNANOSECOND ECL CLOCK WAVEFORMS THROUGH  
MULTICONDUCTOR INTERBOARD SIGNAL CABLES OF VARIOUS TYPES  
(Traces Recorded at Output of Differential Line Receivers)

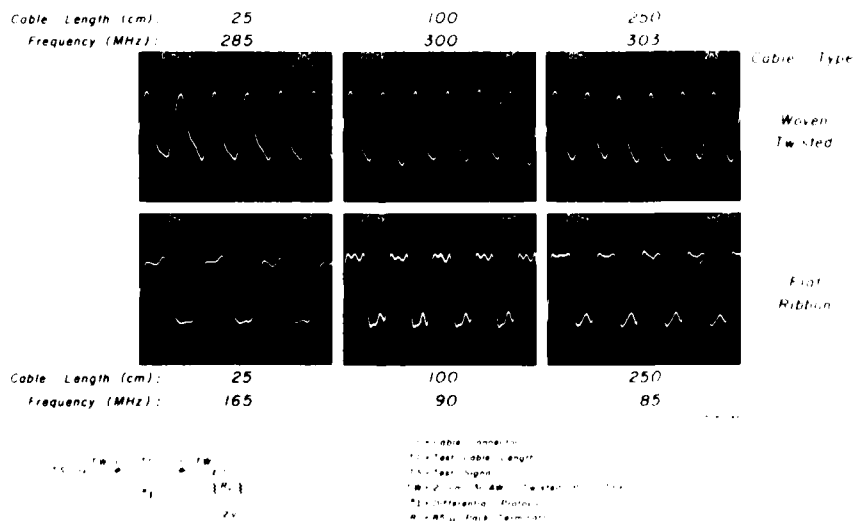


Figure 49

spike transient is sufficient to invalidate use of the cable at these frequencies.

Figure 49 shows similar measurements from differential transmission protocols. Again, at every cable length tested, the upper frequency limit of the twisted cable exceeds that of the flat ribbon cable by a substantial margin, e.g., 285 MHz versus 165 MHz for the 25 cm cable length, and 303 MHz versus 85 MHz for the 250 cm cable length. Comparison of Figures 48 and 49 also demonstrates that the differential transmission protocol outperforms the single-ended protocol regardless of cable type or cable lengths compared. For example, single-ended clock signals transmitted through 250 cm woven twisted cable achieve only 90 MHz maximum rates, compared to 303 MHz maximum rates for the same length and type of cable in the differential mode. This difference is so extreme that the 250 cm woven twisted cable using a differential protocol far exceeds the performance of the 25 cm woven twisted cable employing a single-ended protocol. The differences in maximum usable clock rate through these cables are so much greater for the differential protocol than for the single-ended protocol, regardless of cable type or length, that the differential protocol should always be used, with the clock signal isolated from the remainder of the cable elements by a grounded pair.

Optimum Protocols for Interboard Transmission of Word-Wide Data  
Over Multiconductor Cable

Figures 50 and 51 depict the results of tests of the transmission of word-wide data through adjacent pairs in multiconductor cables. Figures 50 and 51 depict the least significant (and hence the most rapidly toggling) bit in a data word, with transitions occurring at one half the maximum clock rate of the system. The clock waveform was supplied to the transmitting board by a different mechanism to assure that waveform failures in the data bits corresponded to failures of the line transmitter, cable, and line receiver combination, and not to failures of the clocked counter chips (F100136 4-bit counters) employed as the "data generator". Comparison of Figures 48 and 50, with Figures 49 and 51 indicates in every case that for a given transmission protocol, cable type, and cable length, the maximum transmission frequencies for the data bit waveforms are somewhat lower than the maximum transmission frequencies for the clock signals described in the previous section. Transmission rates for data signals are lower than for clock waveforms because of the extra shielding of the clock signals as a consequence of their position at the edge of the multiconductor cables and separation from neighboring signals by a grounded pair. Comparisons between Figures 50 and 51 demonstrate that the woven twisted wire consistently exhibits a higher maximum data bit transfer rate than does the flat ribbon cable, while the differential transmission protocol behaves more uniformly than the single-ended transmission

protocol. Thus, the optimum combined protocol for transfer of word-wide data between logic boards uses a differentially driven woven twisted pair cable. As described previously for clock signal transmission, the performance of the 250 cm woven twisted cable in differential mode is higher than that for the 25 cm woven twisted cable using a single-ended transmission protocol.

The performance of woven twisted pair cable using a differential transmission protocol to transmit both clock and data waveforms was compared with the maximum bit transmission rate for clock and data waveforms achievable for a single-ended protocol through 75 ohm multicoax cable, for a single-ended protocol through 93 ohm multicoax cable, and also for transmission through a pair of RG 174 50-ohm coax cables driven in the dual single-ended mode; all cables were 250 cm in length. The results depicted in Figure 52 were unexpected. For the clock waveform, maximum clock transmission rate was 303 MHz for the woven twisted cable, dropping to 88 MHz for the 75 ohm multicoax in single ended transmission mode, and 24 MHz for the 93 ohm multicoax in single ended transmission protocol. Although the shielding factor of the multicoax cables is very high, reflections and standing waves are more easily created and sustained in the low loss coax cables than they are for the relatively lossy woven twisted cable. Furthermore, since the multicoax was driven in single-ended mode, all reflections and standing waves directly impacted the noise margins of the

MAXIMUM TRANSMISSION FREQUENCIES OF  
SUBNANOSECOND ECL DATA BIT WAVEFORMS DRIVEN  
VIA SINGLE-ENDED PROTOCOLS THROUGH  
MULTICONDUCTOR INTERBOARD SIGNAL CABLES OF VARIOUS TYPES  
(Traces Recorded at Output of Single-Ended Line Receivers  
From Most Rapidly Toggling Bit)

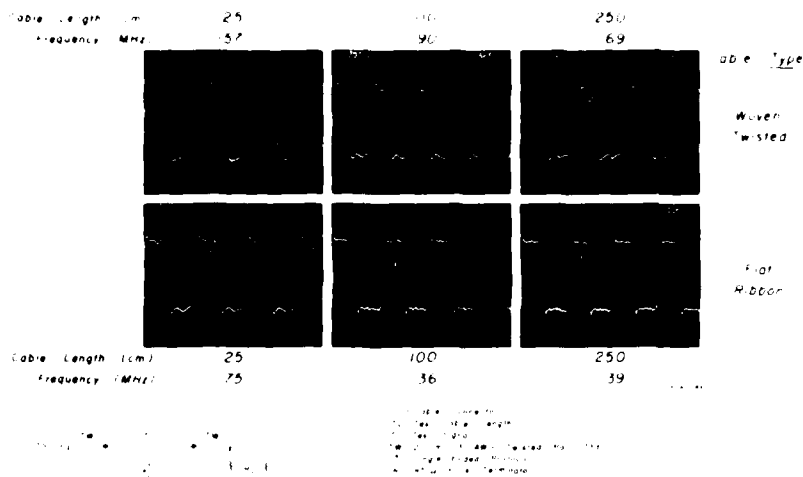


Figure 50

MAXIMUM TRANSMISSION FREQUENCIES OF DIFFERENTIALLY DRIVEN  
SUBNANOSECOND ECL DATA BIT WAVEFORMS THROUGH  
MULTICONDUCTOR INTERBOARD SIGNAL CABLES OF VARIOUS TYPES  
(Traces Recorded at Output of Differential Line Receiver  
from Most Rapidly Toggling Data Bit)

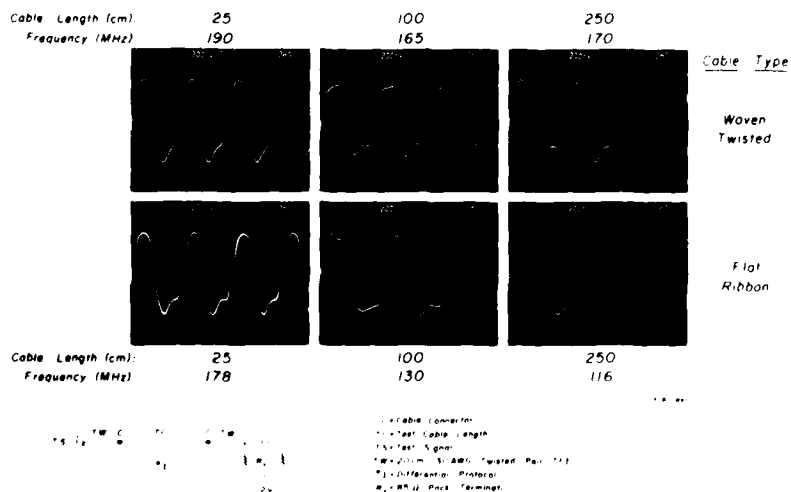


Figure 51



MAXIMUM TRANSMISSION FREQUENCIES OF SINGLE ENDED  
AND DIFFERENTIAL SUBNANOSECOND ECL WAVEFORMS DRIVEN THROUGH  
INTERBOARD SIGNAL CABLES OF VARIOUS TYPES

(250 cm Cable Lengths, Traces Recorded at Outputs of Line Receivers)

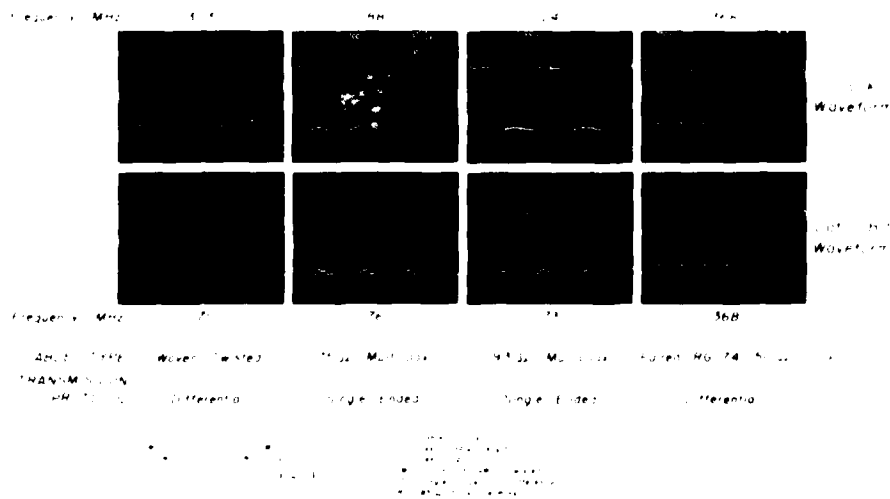
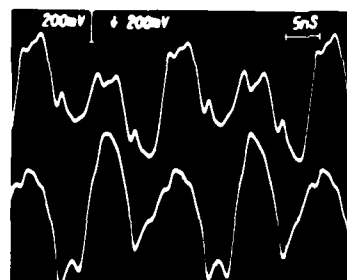


Figure 52

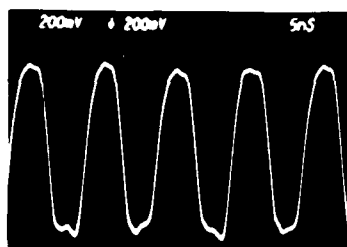
line receivers, causing transient spikes at their outputs (note particularly the third from leftmost panel in the upper row of Figure 52). The 368 MHz maximum performance of the dual single-ended protocol using the paired RG 174 coax cable is even better than that of the woven twisted cable, since the shielding of the true and complement signals is extremely tight, while the common mode rejection capabilities of the differential line receiver are retained. Similar results are seen in the lower row of figures for the data bit waveforms, in which the woven twisted cable in differential mode outperforms the 75 ohm and 93 ohm multicoax cables operated in single-ended transmission mode, and is in turn outperformed by the paired RG 174 cables transmitting in dual single-ended mode.

The importance of the common mode rejection capabilities of the differential transmission protocol can be clearly observed by comparing the upper and lower panels of Figure 53, which depicts simultaneous dual-channel wideband oscilloscope measurements from the true and complement sides of a differential 90 MHz square wave signal transmitted through adjacent

CONTAMINATION OF DIFFERENTIALLY-DRIVEN  
INTERBOARD DATA SIGNAL BY COMMON-MODE  
ABLE NOISE AND RECOVERY OF ORIGINAL WAVEFORM  
via DIFFERENTIAL LINE RECEPTION  
1250 cm Ribbon Cable, 90 MHz Bit Rate,  
Waveforms Measured at Receiver Input Pins



True Signal  
Complement  
Signal



Recovered Signal  
Recovered Signal

wires in a 250 cm flat ribbon cable. Both signals are almost obscured by high levels of noise and reflections, which do not even appear to the eye to be common mode contaminants. The lower panel of this figure was recorded using the A - B input mode of the oscilloscope to simulate the common mode noise rejection capabilities of the differential line receiver.

In summary, it is clear that for any given length of multiconductor cable, a differential transmission, woven twisted cable protocol exhibits the highest bandwidth performance for both clock and data signals and is also the most cost-effective. Clock signals should be isolated at one edge of the cable and separated from data bits in the cable by a grounded pair. With this approach, it is quite feasible to transmit reliable clock signals at frequencies up to 300 MHz between logic panels separated by 8 feet of cable; word-wide data buses may be established over similar lengths at word rates of over 150 MHz. The use of costly multicoax ribbon cables for word-wide data buses appears unnecessary. Lastly, very secure transmission of high speed clock waveforms to multiple logic panels can be accomplished with a dual single-ended transmission protocol employing paired 50 ohm miniature coax cables.

## SECTION 7

### COMPOSITE NOISE MARGINS OF SUBNANOSECOND ECL SYSTEMS FABRICATED WITH COMPONENTS AND PROTOCOLS DEVELOPED IN THIS PROJECT

Before commencing a discussion of composite noise margins of ECL 100K as employed in the Mayo design and fabrication protocol, several definitions of the operating parameters of the ECL 100K logic family are presented:

$V_{BB}$	The threshold voltage of the logic family, equal to $-1.320 \pm .040$ V, with the error representing the lot-to-lot differences observed in 97% of all components.
$V_{IHA}$	The most positive logic HIGH voltage which the input of a logic gate can guarantee to observe as a HIGH signal, equal to $-.880$ V.
$V_{IHB}$	The least positive logic HIGH voltage which the input of a logic gate can guarantee to observe as a HIGH signal, equal to $-1.165$ V.
$V_{OH}$	The nominal output value of a logic gate in the HIGH state, equal to $-.955$ V.

$V_{OHA}$	The most positive output value of a logic gate in the HIGH state due to lot-to-lot differences in manufacture, equal to $-0.880$ V.
$V_{OHB}$	The least positive output value of a logic gate in the HIGH state due to lot-to-lot differences in manufacture, equal to $-1.025$ V.
$V_{OL}$	The nominal output value of a logic gate in the LOW state, equal to $-1.705$ V.
$V_{OLA}$	The most positive output value of a logic gate in the LOW state due to lot-to-lot differences in manufacture, equal to $-1.620$ V.
$V_{OLB}$	The least positive output value of a logic gate in the LOW state, due to lot-to-lot differences in manufacture, equal to $-1.810$ V.

There are a number of acceptable definitions of the noise margin for ECL circuits (Reference 3, Chapter 2). The HIGH state noise margin is usually defined as  $V_{NH} = V_{IHB} - V_{OHB}$  (a negative number) while the LOW state noise margin is usually defined as  $V_{NL} = V_{ILA} - V_{OLA}$  (a positive number). However, as the first source vendor has pointed out, a more appropriate definition of the noise immunity of an ECL system exploits the

fact that a noise contaminant must drive the output of the  $i^{\text{th}}$  gate of a series chain of gates through the  $V_{\text{BB}}$  threshold of the  $(i + 1)^{\text{st}}$  gate for a sufficient duration that the output of this  $(i + 1)^{\text{st}}$  gate itself crosses the  $V_{\text{BB}}$  threshold. For voltages within  $\pm 50$  mV of  $V_{\text{BB}}$ , ECL 100K gates exhibit a gain of approximately 5. That is, if the input signal to the gate is less than  $V_{\text{BB}}$  by, for example, 10 mV, the output of this gate will reach a value 50 mV less than  $V_{\text{BB}}$ . Conversely, an input voltage 10 mV greater than  $V_{\text{BB}}$  will create an output voltage 50 mV greater than  $V_{\text{BB}}$ .

The foregoing comments can form the basis of a realistic technique for the computation of noise margins in an ECL system. If a pulsed noise voltage source is placed on the input of a chain of gates, we may ask how large a positive going voltage  $V_{\text{PN}}$  can be applied at the input without causing a propagating state change through the string of gates (the voltage value so computed will represent the LOW state noise margin; repeating the procedure with a negative-going pulse from a logic HIGH level will yield the HIGH state noise margin). Beginning with the nominal voltage parameters of  $V_{\text{BB}}$ ,  $V_{\text{CC}}$ ,  $V_{\text{EE}}$ ,  $V_{\text{TT}}$ , nominal integrated circuit parameters, etc.,  $V_{\text{PN}}$  will be merely the difference between the nominal values of  $V_{\text{BB}}$  and  $V_{\text{OL}}$ , i.e.,  $V_{\text{PN}} = V_{\text{BB}} - V_{\text{OL}} = -1.320 - (-1.705) = .385$  V. This result is the operational LOW state noise margin voltage if all voltages and integrated circuit parameters are nominal. Each operating voltage and parameter which is not nominal will

in general decrease the noise margin, i.e., decrease the magnitude of the noise pulse which could possibly trigger an erroneous state change. Each of these effects will be considered in turn, both for operational device parameters using vendor-supplied values, and also for noise contaminants and nonuniform power supply voltages, etc., introduced by the Mayo design and fabrication protocol.

If the internal  $V_{BB}$  values of the logic gates are non-typical, noise margins can be adversely affected in two ways. First, at the input of a gate, if  $V_{BB}$  is more negative than it should be, the value of  $V_{PN}$  must be decreased accordingly. The vendor states that  $\Delta V_{BB} = .040$  V, which must be subtracted in its entirety from  $V_{PN}$ . However, changes in  $V_{BB}$  from nominal values also effect the output levels of the gate as well. Noise signals appearing on the input of the  $(i + 1)^{st}$  gate are in effect amplified by the gain  $G$  of the  $i^{th}$  gate. Hence, the tolerable level of  $V_{PN}$  on the input of the  $i^{th}$  gate should be reduced by the value of  $\Delta V_{BB}$  divided by the gain of the  $i^{th}$  gate. Hence,

$$\begin{aligned} V_{PN1} &= V_{PN} - \Delta V_{BB} - \Delta V_{BB}/G \\ &= .385 - .040 - .040/5 \\ &= .337 \text{ V} \end{aligned}$$

If  $V_{OL}$  is nontypical and too positive (i.e., closer to threshold than it should be), the system noise margin will decrease as follows:

$$\begin{aligned}
V_{PN2} &= V_{PN1} - (V_{OLA} - V_{OL}) \\
&= .337 - (-1.620 - (-1.705)) \\
&= .252 \text{ V}
\end{aligned}$$

If there are differences in instantaneous ground potential between the driving and receiving gate, these differences will directly decrease the system noise margin by roughly the peak-to-peak  $V_{CC}$  fluctuations. In the Mayo protocol, we have accordingly paid considerable attention to maintenance of uniform ground potentials. The worst case measured values are  $\Delta V_{CC} = .030 \text{ V}$  peak-to-peak. Hence,

$$\begin{aligned}
V_{PN3} &= V_{PN2} - \Delta V_{CC} \\
&= .252 - .030 \\
&= .222 \text{ V}
\end{aligned}$$

If there are gate-to-gate variations in  $V_{EE}$ , these differences will decrease noise margins by shifting the nominal values of both  $V_{BB}$  and  $V_{OL}$ . However, ECL 100K components employ on-chip compensation to minimize the impact of changes in  $V_{EE}$  on both  $V_{OL}$  and  $V_{BB}$ . In addition, because of the internal designs of ECL 100K gates, the shifts in  $V_{BB}$  and  $V_{OL}$  with changes of  $V_{EE}$  are in opposite directions, nearly cancelling one another. For  $\Delta V_{EE}$  as large as .500 V, the combined decrease in noise margin caused by shifts in  $V_{BB}$  and  $V_{OL}$  following shifts in  $V_{EE}$  is approximately .01  $\Delta V_{EE}$ . In the Mayo protocol, the measured worst case  $\Delta V_{EE} = .040 \text{ V}$ . Hence,

$$\begin{aligned}
V_{PN4} &= V_{PN3} - .01 \Delta V_{EE} \\
&= .222 - .004 \\
&= .218 \text{ V.}
\end{aligned}$$



Fluctuations in  $V_{TT}$ , when the shunt terminated protocol is used, can also directly effect noise margins, by an amount equal roughly to one half the peak-to-peak fluctuation in  $V_{TT}$ . The measured worst case value of  $\Delta V_{TT} = .030$  V peak to peak. Hence,

$$\begin{aligned} V_{PN5} &= V_{PN4} - .5 \Delta V_{TT} \\ &= .218 - .015 \\ &= .203 \text{ V.} \end{aligned}$$

Similarly, fluctuations in the internal bus voltage  $V_{TTT}$  of terminator packs directly effect noise margins by an amount roughly equal to one half their peak to peak fluctuations. The worst case measured noise in the Mayo protocol is  $\Delta V_{TTT} = .050$  V peak-to-peak. Hence,

$$\begin{aligned} V_{PN6} &= V_{PN5} - .5 \Delta V_{TTT} \\ &= .203 - .025 \\ &= .178 \text{ V.} \end{aligned}$$

Note that this noise margin accounts for all sources of signal degradation except for 1) shifts of operating point with temperature; 2) crosstalk introduced through electromagnetic and electrostatic coupling between interconnect wires; and 3) major variations of  $V_{EE}$ ,  $V_{CC}$ , and  $V_{TT}$  between two or more logic panels.

Treating Item 3 first, since the supply voltage variations between logic panels could be far greater than at different

locations on a single logic panel, the composite noise margin for a multiple board system could be substantially compromised. However, use of and rigid adherence to a differential transmission protocol to interconnect logic panels alleviates this potential hazard almost entirely, since individual logic panels are isolated from the instantaneous values of  $V_{EE}$ ,  $V_{TT}$ , and  $V_{CC}$  in differing locations of a large system. Further, the common mode rejection features of the differential line receivers further tend to compensate for variations in  $V_{OL}$ ,  $V_{IL}$ ,  $V_{OH}$ ,  $V_{IH}$ , and  $V_{BB}$  in different components.

Temperature variations between logic panels interconnected with differential protocols are almost entirely compensated by the line driver/line receiver protocol. Although temperature variations between chips on a single board (i.e., local "hot spots") can be minimized by good thermal cooling, some thermal differences are unavoidable. However, ECL 100K is tightly temperature compensated, allowing temperature variations between adjacent components to differ by 85°C with respect to one another, with only very slight shifts in operating parameters. These shifts are already included in the margins stated by the first-source vendor for  $V_{OL}$ ,  $V_{IL}$ ,  $V_{OH}$ ,  $V_{IH}$ , and  $V_{BB}$ .

The remaining contributor to degraded noise margin still to be accounted for is crosstalk between signal lines. Note that the worst case LOW state noise margin  $V_{PN6}$  is only .178 V, a number which appears small to practitioners of TTL design (a

similar number may be derived for the HIGH state noise margin). However, note that for this logic family, the entire nominal signal swing in a low impedance transmission line environment is only .750 V. Hence, the total noise margin, including all deviations except electromagnetic crosstalk, is 23.7% of the total signal swing and 47.5% of the total voltage swing from the logic LOW to the threshold voltage  $V_{BB}$ . However, tests described in Part I, Section 3 of this report indicate that for signal strings using a single-ended-with-ground twisted pair interconnect protocol of even a 25 cm length (a run length which would violate Mayo wiring protocols unless wire-wrappable coax was employed), crosstalk amplitude was only 60 mV peak to peak at 50 MHz and 80 mV peak to peak at 125 MHz. For the computation of noise margin reduction in this worst case example, one half the peak to peak amplitude of the crosstalk voltage  $V_{CT}$  should be employed. Hence, worst case noise margin becomes

$$\begin{aligned} V_{PN7} &= V_{PN6} - .5 V_{CT} \\ &= .178 - .040 \\ &= .138 \text{ V.} \end{aligned}$$

This noise margin, including worst case wiring crosstalk, still retains .138 V LOW state noise margin, i.e., 18.5% of the total signal swing and 37% of the range between the nominal logic LOW level and  $V_{BB}$ , thus retaining a substantial noise immunity safety factor for any other disturbances. Hence, the Mayo-developed

design protocols, in conjunction with the ECL 100K logic family, provide a stable, reliable design and fabrication technology for ultra high speed systems.

## SECTION 8

### OPERATING CHARACTERISTICS AND PERFORMANCE OF ENGINEERING PROTOTYPE DEMONSTRATION TEST CIRCUITS

To test the performance capabilities of the logic panels, terminator components, and wiring protocols developed in this project, three engineering demonstration test circuits were designed in an increasing scale of complexity and parts count. The First Engineering Demonstration Test Circuit, consisting of approximately 20 integrated circuits and depicted in schematic form in Figure 27, has already been described in detail; operational measurements from this circuit have been presented in Figures 28 and 29. This test circuit was the first verification that the combination of specially designed components, logic panels, and wiring protocols would perform as intended with very low levels of system noise and crosstalk. Test results from this circuit also indicated possible performance limitations resulting from the electrical characteristics of the dual in-line packages, as has been documented in previous sections of this report.

The Second Engineering Demonstration Test Circuit verified the performance capabilities of systems containing 75-100 integrated circuits, executing large numbers of arithmetic operations at clock rates above 100 MHz. The design chosen for this Second

Demonstration Test Circuit was a small 9-element direct convolver-correlator capable of performing convolution or correlation operations on data vectors of any length, with element precision in the input data vector of six bits. The design of the direct convolver-correlator is schematized in the lowermost panel of Figure 54. The design of the convolver-correlator was deliberately optimized for symmetric, linear phase filter kernels,

**DIRECT HARDWARE IMPLEMENTATION OF  
DISCRETE CONVOLUTION SUM WITH MODIFICATIONS  
FOR SPECIFIC KERNEL CHARACTERISTICS**

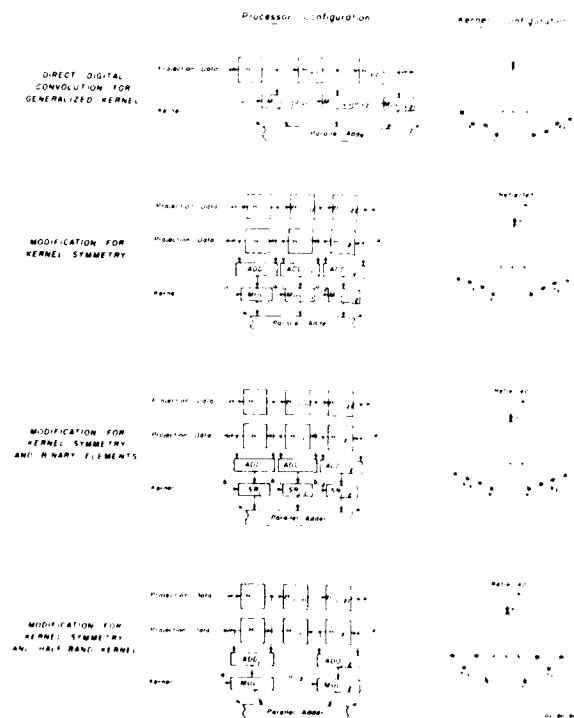


Figure 54

since it has recently been demonstrated that any symmetric filter kernel may be converted into an equivalent form in which all elements of the kernel are of the form  $\pm 2^{-n}$ ,  $n$  any integer (References 4,5,6). Linear-phase filtration and correlation are operations widely employed in digital signal processing, frequently requiring operation at real time clock rates above 100 MHz.

The backplane and chassis of the Second Engineering Demonstration Test Circuit are depicted in Figure 55. At a clock

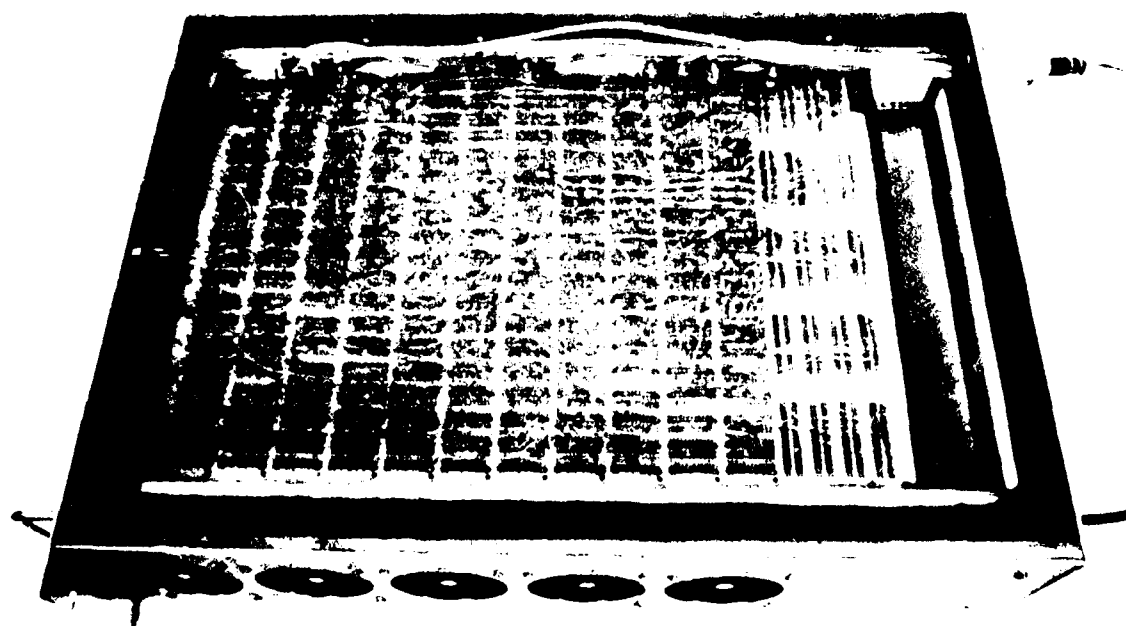


Figure 55

SECOND ENGINEERING DEMONSTRATION TEST CIRCUIT MOUNTED IN CHASSIS (BACKPLANE VIEW). NOTE INTEGRAL COOLING FAN AND MULTIPLE OFF-BOARD CABLE CONNECTORS.

rate of 125 MHz, the processor accepts a new input operand and produces a processed output operand every 8 nsec—secondly, fifteen data elements are processed simultaneously in four stages of the computer architecture of this convolver-correlator exceeds that of present generation programmable array processors by a factor of possibly  $10^3$ , executing one billion 18-bit arithmetic operations and two million 18-bit precision binary shift operations per second. The high speed oscilloscope traces of Figure 56 depict single bit-lines at various locations within the functioning processor, including outputs from a data register, from one of the binary shift networks, from a fixed precision adder, and from the final output

*DIRECT CONVOLUTION FILTER PROCESSOR  
FABRICATED WITH SUBNANOSECOND ECL  
(125 MHz System Clock; 6-Bit Input and 18-Bit Output Data;  
9 Elements; Wire Wrap Interconnects)*

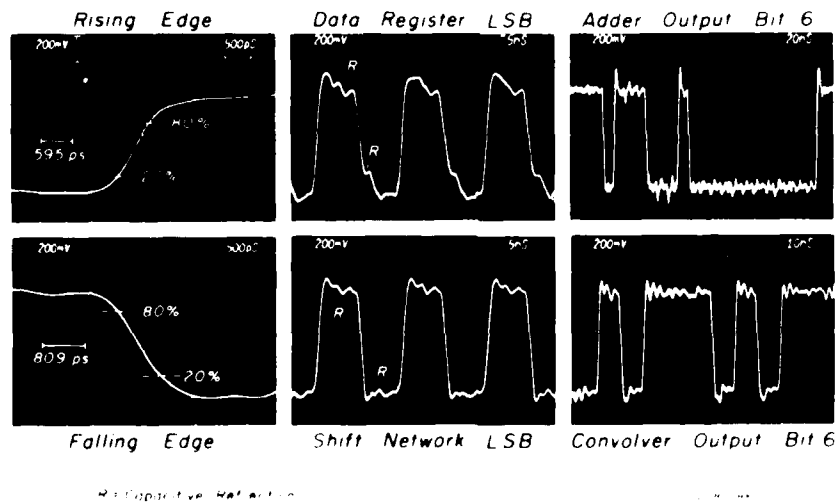


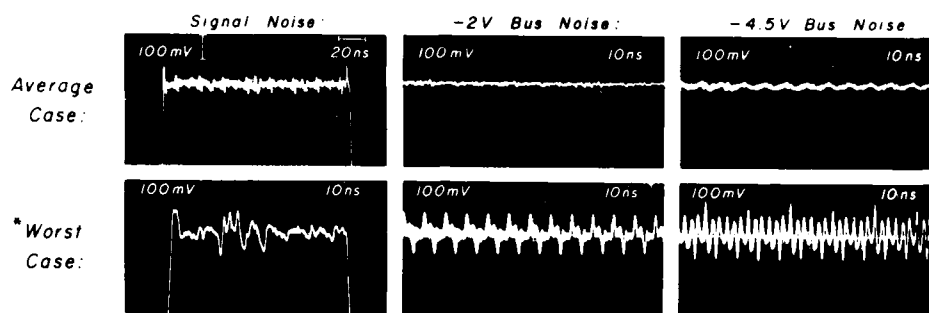
Figure 56



of the convolver-correlator. The individual signal traces are relatively free of noise and reflections (the reflections are indicated in several of the panels by the letter R). The leftmost panels of Figure 56 display typical rising and falling edges of an arbitrarily selected waveform, of 595 psec and 809 psec respectively. Although both edge times are subnanosecond, they are not identical since the driving gate pulls the line HIGH, the terminator pulls the line LOW, and the output impedances of the gate and terminator are quite different (roughly 7 ohms and 75 ohms respectively). This lack of edge symmetry motivated an earlier warning that the phase timing of a square-wave clock signal when traversing several layers of drive gates can become nonsymmetric in its true and complement phase timing.

Figure 57 shows a series of composite noise measurements made of the convolver-correlator circuit while in operation at the 125 MHz clock rate. The upper row of images depict an expanded view of the composite noise on the logic HIGH level of a signal waveform (leftmost panel, 80 mV peak-to-peak), of the -2 V bus noise (30 mV peak-to-peak), and of the -4.5 V bus noise (40 mV peak-to-peak) respectively. These are typical noise levels commonly observed throughout a functioning circuit, i.e., the average case. To create the worst case composite noise levels depicted in the lower row of images, a signal was driven to a pin on an otherwise empty socket location, then terminated at a terminator pack. However, the empty socket

DIRECT CONVOLUTION FILTER PROCESSOR FABRICATED  
WITH SUBNANOSECOND ECL  
(125 MHz System Clock; 6-Bit Input and 18-Bit Output Data;  
9 Elements; Wire Wrap Interconnects)



\*Measured at Empty Socket,  
with No Decoupling

Figure 57

location also contained no decoupling capacitors (a serious violation of the interconnect protocol). Representing worst-case conditions, these noise levels are a combined value of 180 mV peak-to-peak on the logic HIGH level of the signal, 150 mV peak-to-peak on the -2 V bus, and 220 mV peak-to-peak on the -4.5 V bus (the LOW to HIGH signal transition range of 100K ECL is 800 mV). These measurements reconfirm the earlier experimental finding that each integrated circuit exists in its own local electrical environment. In this case, removal of the decoupling capacitors from the empty socket location

resulted in the creation of a localized "island" on the logic panel displaying very high noise levels, even though similar noise measurements on an immediately adjacent and properly decoupled socket less than 0.5 inch away displayed "average case" noise levels nearly identical to those of the upper row of panels in Figure 57.

The Second Engineering Demonstration Test Circuit was also used as the test vehicle structure for the noise, cross-talk, and dispersion measurements depicted in Figures 14, 15, and 18 through 25.

No attempt was made to achieve maximum pipelining capability in the design of the convolver-correlator test circuit; a minor redesign to include an additional rank of pipelining registers could have achieved a maximum clock rate of approximately 150 MHz, or 20% greater than that of the present system. However, the performance of the Second Engineering Demonstration Test Circuit was considerably lower than our design specification; based upon the worst case propagation delay estimates published by the first-source vendor for these components, we expected correct operation to a clock rate of at least 200 MHz. Part type by part type measurements of the propagation delays of the 24-pin Cerdip packages were then carried out which demonstrated that the performance of the ECL components was poorer in every case than the vendor-published worst-case device timing. As indicated previously, the performance degradation

of these components appears to be caused by the series inductances and shunt capacitances of the Cerdip lead frame structures. The performance of the Second Engineering Demonstration Test Circuit demonstrated that maximum performance of the ECL dice probably cannot be achieved without conversion to leadless chip carriers.

The Third Engineering Demonstration Test Circuit is a dual logic panel system consisting of nearly four hundred integrated circuits, which is the primary test vehicle for verification of noise and crosstalk problems and interboard cabling protocol compatibility in a large system operating at moderate clock rates (20-40 MHz). This system is an interface unit between a high speed time-base-correcting A-D/D-A converter and a special purpose communications computer which preprocesses the digital data stream to and from the converters. Figure 58 shows the two chassis, each containing a logic board and cooling fans, with woven twisted pair interboard cables exiting through the rear of each. This dual board system was the vehicle for operational testing of interboard data transmission protocols, and for methods of clock signal distribution to multiboard systems. The results of these studies have already been discussed in conjunction with Figures 39 and 44 through 53. Figure 59 is a closeup photograph of the wired backplanes of one of these two logic boards, clearly showing the twisted pair interconnects. Note that several of the twisted

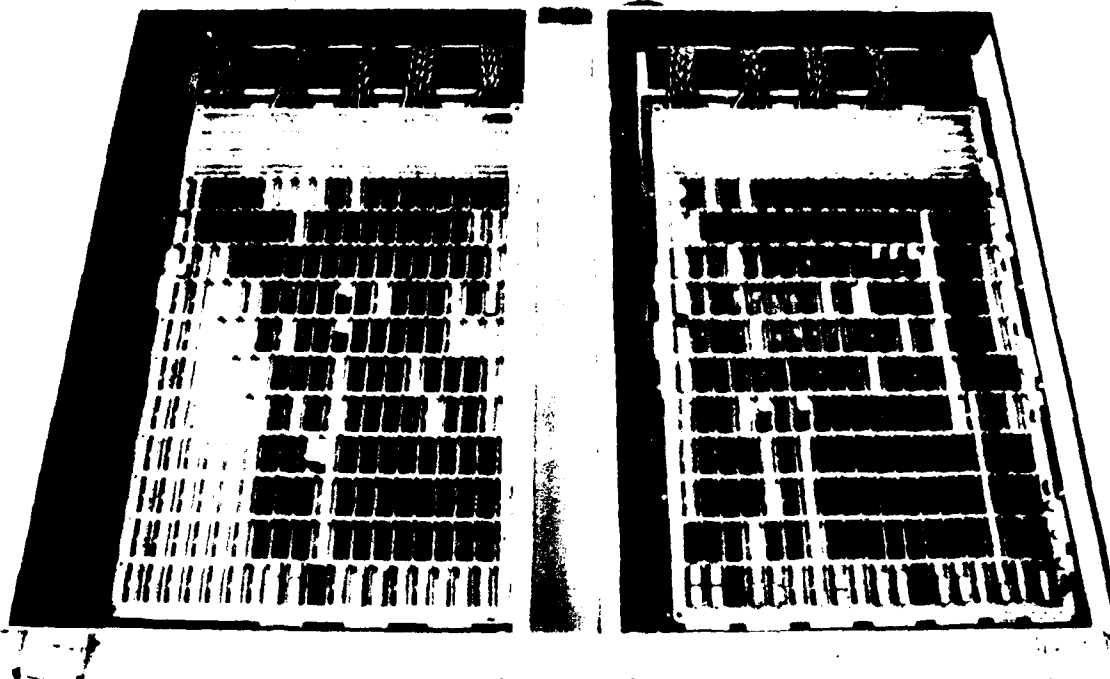


Figure 58

DUAL BOARD SYSTEM COMPRISING THE  
THIRD ENGINEERING DEMONSTRATION TEST CIRCUIT

pair runs are several inches in length; however, as noted earlier, the moderate clock rates (20-40 MHz) of this system and the high noise resistance of the wiring protocols allow proper operation with extremely low composite noise levels. Other than occasional wiring errors arising during the physical fabrication of the logic boards, no unexpected technological problems were encountered in the development of this system. This



Figure 59

BACKPLANE WIRING OF  
THIRD ENGINEERING DEMONSTRATION TEST CIRCUIT

two board circuit design was also employed as a verification vehicle for the computer-aided design (CAD) system for sub-nanosecond ECL also developed under this contract, which will be described in Part II of this report.

## Design of Synchronous and Asynchronous Systems

In the development of large digital systems, the engineering staff must choose between fully synchronous (clocked) designs, asynchronous (handshake) designs, or combinations of both. At clock rates of 20 MHz or less, TTL-based systems can use either design philosophy. However, as system throughput rates are increased, and particularly in those cases in which subnanosecond ECL implementations are employed, asynchronous systems become progressively less attractive. This occurs because by definition, critical events occur in asynchronous systems at random moments in time, making repetitive testing and reliable identification of system faults with respect to repeated time increments virtually impossible. Further, subnanosecond ECL components are capable of responding (correctly or incorrectly) to pulses of only 2 or 3 nsec duration, which are so brief that presently available diagnostic equipment often is not even capable of demonstrating their occurrence. A detailed comparison of the advantages and disadvantages of the two approaches is beyond the scope or intent of this report; however, based upon experience with a half dozen large systems fabricated both in ECL 10K and ECL 100K, we believe that high speed systems, especially if fabricated with subnanosecond ECL, should rely upon totally synchronous designs. Not only is this discipline enforced upon our engineering staff, but the ECL computer aided design (CAD) programs described in Part II of this report are designed to reject asynchronous logic as

a fundamental violation of the subnanosecond ECL design rules. This conclusion must be considered one of the most fundamental design rule results of the Mayo studies, which should not be violated if processor architectures operating at clock rates in excess of 50 MHz are to perform reliably.



## SECTION 9

### TEST EQUIPMENT APPROPRIATE FOR USE WITH SUBNANOSECOND EMITTER COUPLED LOGIC

Test equipment to be used for subnanosecond ECL systems must be selected with a thorough understanding of the fast wavefronts and low impedance characteristics of this logic family. As demonstrated in Figure 33, even the act of probing a signal string for test purposes can markedly alter its operational characteristics. The use of test equipment not appropriate for the ECL environment can markedly alter the actual operation of entire systems, or cause an incorrect assessment of their operation.

### Clock and Word Generators and Universal Counter/Timers for Subnanosecond ECL Systems

Selection of an appropriate pulse generator to provide the system clock waveform for circuits under bench test condition is straightforward. The Hewlett-Packard Model 8080A word/pulse generator system allows a variety of clock generator and amplifier modules to be selected according to the desired speed regime and fanout. The Model 8091A rate generator, 8092A delay generator, and a pair of 8093A driver amplifiers are used here to produce a two phase clock signal at rates from 100 Hz to 1 GHz, with tunable delay between phases in 10 psec

increments. The Model 8081A plug-in produces a single phase clock signal from 100 Hz to 300 MHz at a somewhat lower cost. Addition of a Model 8084A Serial Word Generator allows programmable word generation at rates up to 300 MHz. These units adequately drive 50 ohm loads, and have preset switch positions to drive the subnanosecond ECL logic HIGH and LOW levels of -0.9 and -1.7 volts respectively.

The Hewlett-Packard Model 8016A 9-bit parallel word generator allows up to 64 parallel 9-bit bytes to be transmitted continuously or in single bursts; the unit can also be programmed to transmit a single 256-bit serial code. TTL or ECL voltage output levels are both available, either in single ended or differential mode. Although this device has proven to be adequate for subnanosecond ECL systems, there is a major pitfall if operated without some care. The unit allows variable phase control for all even-numbered data bits; however, if any of the phase delay settings are inadvertently made greater than the interclock interval setting, the output waveforms of all bits behave in an irregular and unpredictable manner: the waveforms convert rapidly back and forth between full frequency and half frequency configurations, resulting in erroneous inputs to the circuit under test. This problem can be alleviated by very careful setup of the 8016A generator prior to initiation of tests. An additional limitation is the unit's inability to operate in byte-parallel mode at clock rates greater than 50 MHz, a very severe restriction considering that the ECL

system under test can often operate in word-parallel mode at clock rates above 200 MHz. We are not aware of a word generator similar to the 8016A from any other vendor which operates at a higher clock rate, a serious deficiency in the regime of test equipment available for this logic family (several Hewlett-Packard Model 8084A serial word generators could be used in parallel, but at a prohibitive cost). The 2 nsec rise and fall times of the Model 8016A word generator are marginally adequate for subnanosecond ECL, but since the word generator is not capable of operating at clock rates above 50 MHz, the point is probably moot.

The availability of a flexible ultra high speed universal counter-timer can often be of considerable benefit in initial operational verification and maintenance support of systems fabricated with subnanosecond ECL. We have very recently acquired, and are presently testing, a Hewlett-Packard Model 5315/B 100 MHz Universal Counter. Of several available factory-supplied options, Option 003 increases the frequency counting range from 100 MHz to 1 GHz; the Mayo unit has this option installed. Initial tests verify that the unit is accurate and reliable up to approximately 1 GHz when tested against a Hewlett-Packard Model 8080A pulse generator. Early tests of the unit in actual measurements of ECL 10K circuitry appear to be satisfactory. The 5315B has not been tested at the time of this writing on operational ECL 100K systems. Until further evaluation has been carried out, concerns regarding possible hypo- or hypersensitivity of the adjustable threshold level of the

unit will persist (based in part upon negative experience with similar features of the Hewlett-Packard Model 1600S Logic Analyzer described below).

#### Logic State Analyzers for Subnanosecond ECL Systems

The tremendous proliferation of logic state analyzers in the past few years have almost exclusively been directed to the requirements of designers of TTL or MOS low speed micro-processor systems, and in some cases to TTL-based SSI and MSI integrated circuit designs. Two logic state analyzer units oriented to higher speed systems are in use in our laboratory. The Hewlett-Packard Model 1600A/1607 logic state analyzer (often referred to as the 1600S), though introduced several years ago, is still available, and, with minor modifications, can be used in an ECL environment. Although this device was originally intended for use with TTL systems, both the 1600A and 1607 contain front panel threshold level switches which, when placed in the VARIABLE position, allow screwdriver adjustment of reference threshold levels within the unit to those of ECL. However, we identified two design deficiencies in these units, one in the probe pod and one in the logic analyzer mainframe, which cause the internal reference voltage buses to be badly contaminated by system noise. This, in turn, creates instability in the offset and gain circuits in the 1600S, resulting in a degradation of the apparent noise margins of the ECL logic, and causing the 1600S to false-trigger and report errors in the

system under test. Design modifications have been developed in our laboratory for both the logic probe pods and the logic analyzer mainframes to control reference bus noise, which can be obtained from Mayo Foundation upon request. With these fixes, the 1600S can be considered a marginally adequate unit for use in a subnanosecond ECL environment.

The most stable and reliable logic analyzer unit available commercially for use with subnanosecond ECL is the Tektronix 7D01/DF2 (or 7D01/DF1) logic analyzer/data formatter. Like the Hewlett-Packard 1600S, this unit has a front panel threshold switch and a screwdriver adjustable variable threshold. Unlike the 1600S, however, these threshold levels can be set reliably and do not need continuous adjustment thereafter. The 7D01 logic analyzer is limited in the ECL environment by its inability to operate in synchronous sampling mode at externally supplied clock rates above 50 MHz, and then only when sampling four channels; the device also has a 100 MHz sampling mode when sampling up to four channels referenced to its internal free running clock. However, use of the internal clock mode tends to generate "sliver pulse" measurements whose validity is difficult to evaluate. In addition, the input impedance of the probe pods is somewhat lower than desirable. The shunt capacitance of several pF of the probe pod leads, and the low input impedance and accompanying signal string loading behavior resulting therefrom are serious, though not sufficient to halt the operation of a properly wired signal string, particularly if the test

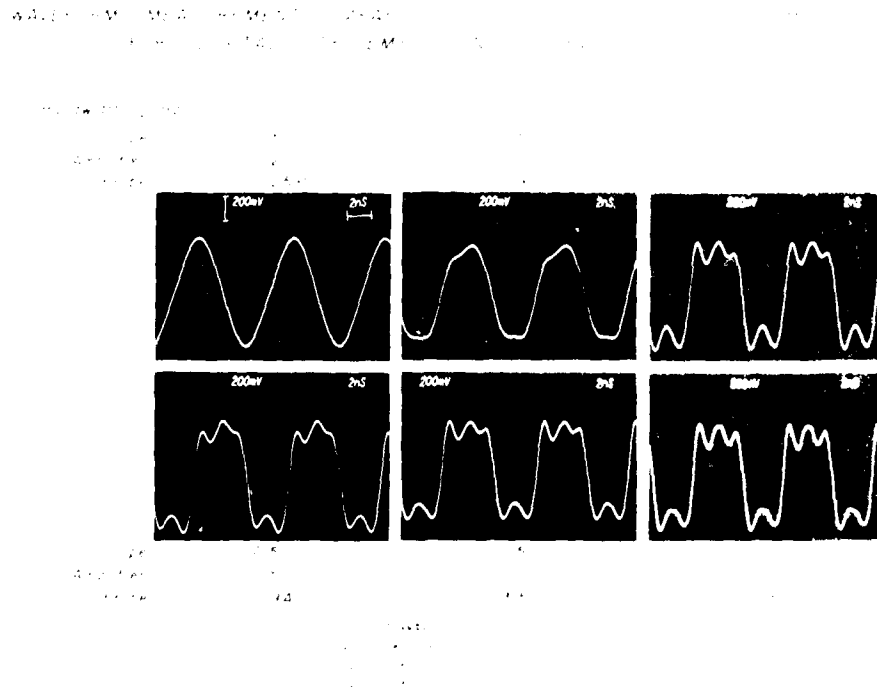
lead is placed on the terminator of the signal string to be measured. However, marginally operational signal strings with incorrect termination, an excessive number of destination modes, or a faulty source gate can be adversely effected. The vendor of the 7D01/DF2 logic analyzer is aware of the insufficient speed capability of the 7D01, particularly its inability to detect and identify extremely short sliver or runt pulses of durations less than 10 nsec; this limitation has been partially alleviated by the development of the Model DL2 Digital Latch plug-in unit to operate in conjunction with the 7D01. The problem of low shunt impedance in the probe pods is also under investigation by the vendor. However, the vendor states that there is insufficient demand for logic state analyzers of higher speed capability and lower circuit loading characteristics to allow a rapid solution of the loading and speed problems, although the technology is now available to solve both.

Although we have not tested the Biomation Model K-100 logic analyzer, the specification sheets for this unit do not indicate any significant performance improvement of the Biomation unit over the Tektronix 7D01/DF2 or 7D01/DF1.

#### Wideband Oscilloscopes and Test Probes for Use With Subnanosecond ECL Systems

Figures 60 and 61 depict the results of measurements of a typical signal string in an operational prototype subnano-

second EFL circuit which were performed with various combinations of oscilloscope mainframes, vertical amplifiers, and oscilloscope probes. To create a realistic test environment, the signal string from which the test signal was deliberately selected to exhibit some degree of distortion and wavefront contamination. Figures 6 through 11 show the results of eight such combinations of test equipment and the bandwidths of the elements in the test system are presented beside each panel in the figures.



WAVEFORM MEASUREMENT CAPABILITY OF OSCILLOSCOPE INSTRUMENTATION  
FOR DIGITAL SYSTEMS USING SUBNANOSECOND FCL

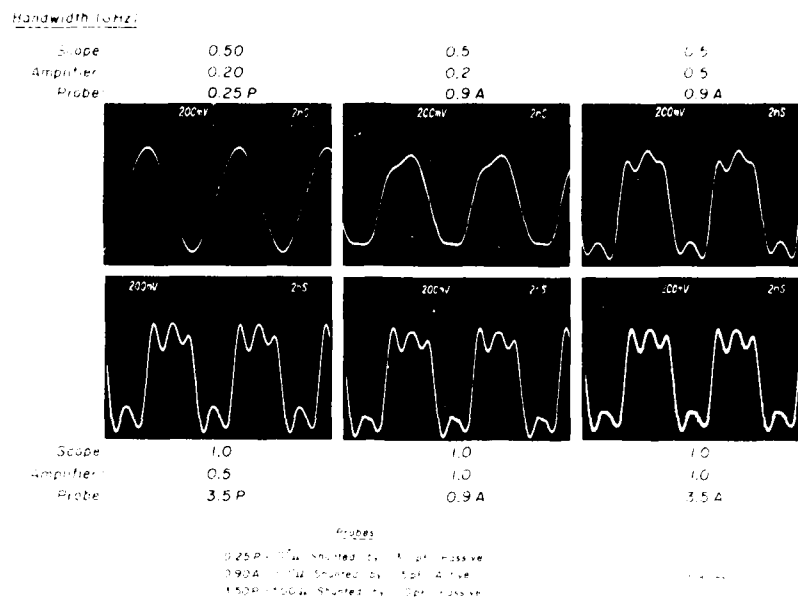


Figure 61

The combination of mainframe, vertical amplifier, and probe with the highest aggregate bandwidth is depicted in the extreme lower rightmost panel of both figures, as the standard by which the other panels may be compared. As demonstrated by the upper leftmost panel of Figure 60, it was unnecessary to include an oscilloscope mainframe whose upper half-power bandwidth was less than 500 MHz (e.g., the Tektronix Model 7704A 250 MHz mainframe), since waveform degradation would have been excessive. Progressing from left to right in the upper and then the lower rows, a combination of oscilloscope mainframes,



amplifiers, and probes were tested displaying bandwidths from 500 MHz, 200 MHz, and 300 MHz respectively, to similar units with 1 GHz, 1 GHz, and 3.5 GHz bandwidths respectively. Waveform conformations in the upper leftmost two panels of both figures are clearly unrepresentative of the behavior of the circuit. However, the upper rightmost panel demonstrates that for facilities not performing laboratory-grade research to develop new fabrication protocols, the combination of a 500 MHz mainframe oscilloscope, a 500 MHz vertical amplifier plug-in unit and a 900 MHz active probe or 3.5 GHz passive probe (see following discussion) result in satisfactory reproduction of waveform content. If laboratory grade research is to be performed to develop new ECL protocols, or if entirely new devices are to be investigated for the first time, the 1 GHz oscilloscope mainframe and vertical plug-in units should definitely be employed.

#### Probes

Figure 60 demonstrates that amplifier and test probe overshoot characteristics and the loading of the signal string caused by the probe create considerable differences in the appearance of the measured waveform and in waveform conformation respectively. Note particularly the first overshoot peak immediately following the rising edge of the waveform in the upper rightmost panel, measured with a 3.5 GHz passive probe, and the first overshoot peak following the rising edge of the

waveform in the lower leftmost panel, measured with a 0.9 GHz FET-input active probe. The overshoot peak in the upper rightmost panel is generated by the substantial overshoot characteristics of the 0.9 GHz active probe, as measured in this laboratory and confirmed by the manufacturer of the probe. The DC input resistance of the active probe is  $10^{10}$  ohms, with an input shunt capacitance of 3.5 pF; if a 10X auxilliary barrel is added, the DC input resistance remains  $10^{10}$  ohms, while the input shunt capacitance decreases to 1.5 pF. The best alternative to the active probe is the passive probe, designed for sampling applications, which exhibits a DC resistance of 50 ohms in series with the 450 ohm input impedance of the wideband amplifier units for which this probe is intended.

Although exhibiting much lower DC input resistance than the active probe, the shunt capacitance of the 3.5 GHz passive probe is 1.5 pF, i.e., equal to that of the active probe with the 10X auxilliary barrel in place. In addition, the overshoot response of the passive probe is negligible. In a subnanosecond ECL environment with signal frequency components of 1 GHz and greater, the shunt input capacitance of the probe is the dominant portion of its input impedance. A shunt capacitance of 3 pF placed across the string under test is an equivalent load of slightly greater than 50 ohms. If a probe with a 3 pF input capacitance is placed at the terminator resistor, the line termination will be changed from a value of, for example, 75 ohms, to approximately 30 ohms, thereby considerably underterminating

the line and creating large negative wavefront reflections at the terminator. If a probe with a shunt capacitance of 1 pF is positioned at the terminator, the 150 ohm equivalent shunt impedance of the probe in parallel with the 75 ohm terminator resistor will be in the neighborhood of 50 ohms, also underterminating the 75 ohm transmission line interconnect though not to nearly as great a degree. The loading effects of the logic probes on signal timing performance can easily be observed in panel C of Figure 33, in which a 500 ohm passive probe with a 1.5 pF input shunt capacitance was placed on node 2 while a TDR measurement of the unpopulated logic string was carried out. Panel D of Figure 33 demonstrated that the wavefront delay of the unbalanced divider circuit caused by the probe (34 millirho-nsec) is more than twice that of an empty leadless chip carrier. Hence, it is clear that the measurement probes are themselves part of the measurement problem. This example demonstrates that the probing of ECL test strings with presently available probes always causes distortion of the actual signal level. As demonstrated by the data of Figure 33, placement of a passive probe with even a 1.5 pF input capacitance on any of the nodes of a 100 picosecond delay logic string will not only cause a considerable impedance discontinuity and consequently signal wavefront reflections emanating from that location.

Discussions with engineers at Tektronix, Inc., have indicated recent improvements in the design of both the active and

passive probes can be achieved which would partially alleviate these loading problems. Tektronix is currently investigating two new probes for use with high speed ECL devices. The active probe under study will employ a gallium arsenide MESFET amplifier in the probe tip, with an input resistance in the  $10^{10}$  ohm range, an input shunt capacitance of less than 1 pF, and minimal overshoot characteristics. This probe is expected to be ready for initial testing by the first quarter of 1981. The second probe, a passive device, will be similar to the presently available 3.5 GHz passive probe now used routinely for ECL in our laboratory; however, the voltage reference of the new probe will be changed from ground to the threshold voltage for subnanosecond ECL, that is, a  $V_{BB}$  of approximately -1.3 volts. The input shunt capacitance of this probe will remain in the 1-1.5 pF range, but its equivalent DC resistance will be considerably greater than 500 ohms. The  $V_{BB}$  biasing of the probe will limit DC current flow in the new probe to approximately 25% that of the present passive probe, for an equivalent DC resistance of approximately 1500-2000 ohms. Tektronix, Inc., will allow the Mayo Foundation research group to test early engineering models of these new probes; we hope to report their performance in the next yearly progress report.

## PART II

### A COMPUTER-AIDED DESIGN PACKAGE FOR SUBNANOSECOND ECL SYSTEMS

#### Introduction

The Mayo Emitter Coupled Logic (ECL) Computer-Aided Design (CAD) software package is a set of software modules which provide conceptual tools for the specification of a logic design, the verification of that design, and finally, for its documentation. The primary reasons for using a CAD-based system design approach include:

- 1) Reduction of the paperwork burden on the designer, allowing him to concentrate on creative design tasks.
- 2) Improvement of the efficiency and speed of the logic design and layout process by provision of intermediate design verification data, thereby allowing early detection of design and layout errors.
- 3) Minimization of system checkout effort by provision of comprehensive documentation aids.
- 4) Improvement of reliability by constraint of new systems designs to a single, comprehensive layout and interconnect protocol.
- 5) Improvement of system maintainability by the creation of uniform, comprehensive design documentation at a very high level.

The overall CAD package has been designed with a modular, hierarchical schema to reduce the level of complexity of any given software module, to subdivide the task of software system generation into a logical set of steps, and to permit easy reconfiguration of the software. It is planned that modules will be added to the CAD package on an ongoing basis to provide increasingly stringent testing of new system designs. Such modifications can be carried out in a straightforward manner because the software package contains a general framework into which can be included a variety of software substructures.

The Mayo-developed CAD is oriented towards the design of special purpose high speed digital processors, the logic for which will be installed on large wire wrap socket boards (multi-layer printed circuit boards are too costly for one-of-a-kind designs, generally requiring a lengthy development cycle). Subnanosecond emitter coupled logic is exploited to achieve high component speed. However, the use of subnanosecond ECL requires rigorous design rule checking effort to concentrate upon a limited set of critical design schemas (protocols). The complexity of such a rigorous transmission line interconnect and termination methodology, detract from the advantages of ECL from the designer's point of view because they are unrelated to the actual logic design. Delegating the details of these interconnect protocols to an interactive CAD package is clearly of great assistance to the designer.

The first two generations of CAD at Mayo (a TTL CAD package developed in 1973 and an ECL 10,000 CAD system written in 1975) were primarily documentors and net optimizers, and possessed few of the capabilities envisioned for this third generation CAD. The third generation CAD is a completely new software package which capitalizes and enlarges upon concepts and capabilities developed for the earlier software, but which also adds a considerable number of completely new functions. Several painful lessons learned in the earlier CAD efforts, as well as a number of factors known from the beginning of the subnanosecond ECL CAD project greatly influenced the direction of the present effort. The following issues served as constraints on the development of the subnanosecond ECL CAD package:

- 1) The method for specifying the logic board design must permit a wide variety of layouts.
- 2) Component specification algorithms must be sufficiently flexible to tolerate evolutionary and radical changes in components, packaging, and technology.
- 3) The algorithms by which board connections are specified must provide design support for an internally consistent and comprehensive set of interconnect protocols required for ECL system fabrication.
- 4) Since the design check rules are nontrivial in complexity, the rule specification capability must be very extensive and the operational flexibility considerable.

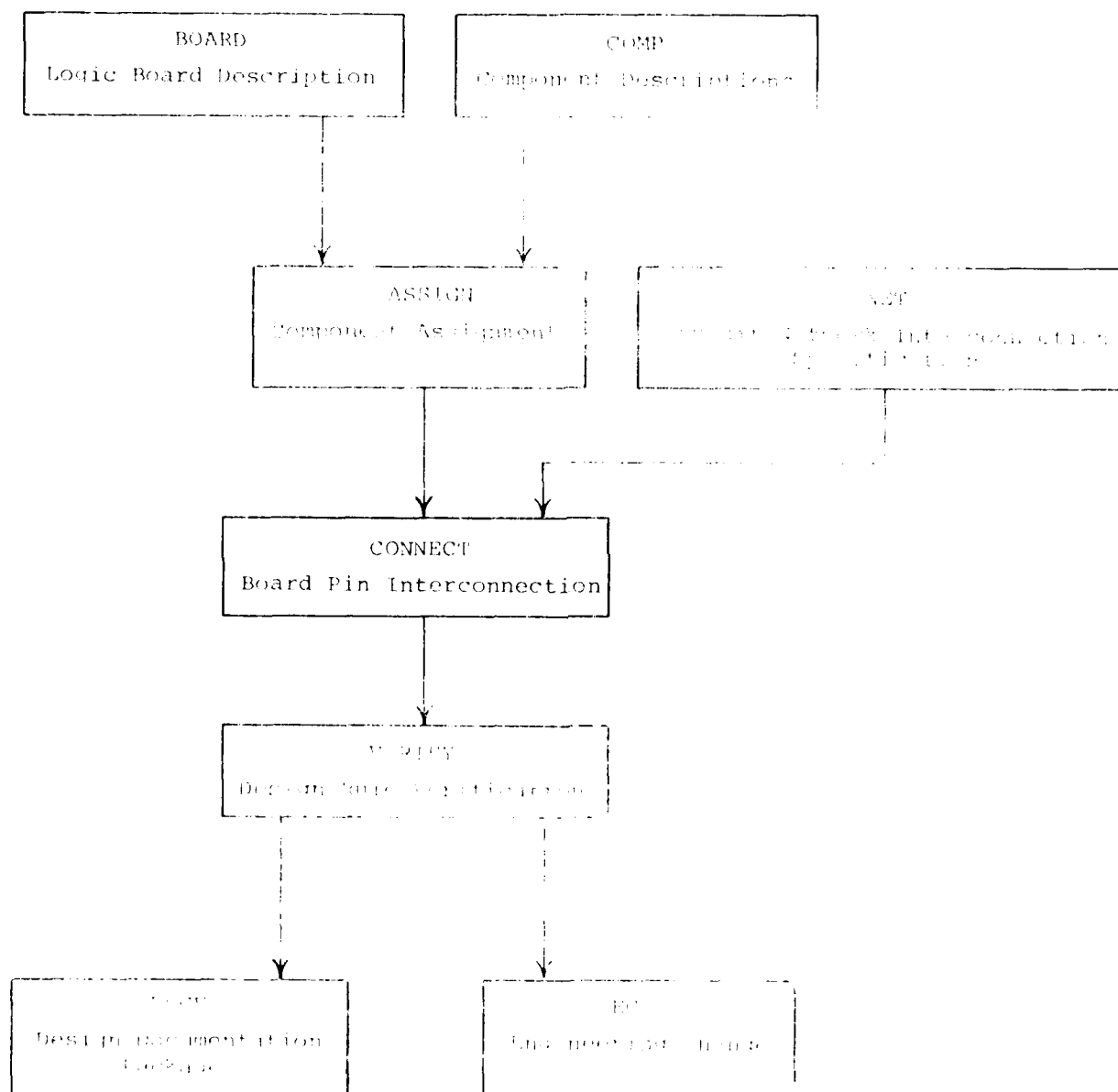
- 5) The design check rules are not static, but continue to evolve with experience and as a result of changing device technologies; the method of rule specification must therefore be flexible.
- 6) Various design and documentation methods, previously established in our work with TTL and ECL 10K, must be maintained.

Several factors related to the characteristics of the computer systems available for the development and eventual routine execution of the CAD have greatly influenced the software structure as well. The subnanosecond ECL CAD has been developed under the assumptions that: 1) available core for program execution will be small; 2) available disk storage will be large; 3) job run times may be limited during the working day in a batch or multi-batch environment; and 4) the only readily available and highly transportable higher-level language is ANSI FORTRAN (this assumption has imposed a number of very stringent programming limitations).

### System Overview

A block diagram description of the CAD package appears in Figure 62. The block interconnections do not fully describe the data flow, but rather indicate the general interrelationships between the modules. Following the presentation of a brief description of each block (module), a more complete definition of each will appear in succeeding sections.





Computer Aided Design (CAD) Process

Figure 1

- BOARD - A wire wrap socket board is described. The board may have any configuration. A record is created for each pin which contains its physical and electrical attributes, including its x-y coordinates, location name, and power/ground plane connections, if any.
- COMP - Components (IC chips, switches, discretes, cable connections, etc.) are described and entered into a component dictionary, which contains component names, pin coordinates, pin numbers, and a variety of physical and electrical component attributes.
- NET - The circuit network (pin interconnections) is specified. A group of pins interconnected by wire (Net) is given a name; signal sources and destinations are then specified.
- ASSIGN - This software module uses the component dictionary to concatenate component information into the records defined in the BOARD module, an operation which is analogous to installation of a component on the circuit board.
- CONNECT - The records created by BOARD are linked together. The result of the linking operation is a group of pins and an order in which they will be interconnected. The group specification was previously

generated by the module called NET, while the ordering of the pins is performed by a connection optimizer within CONNECT.

VERIFY - Design rule verification is performed by applying a set of rules to each net specified in the NET module. The rules operate upon the attributes previously assigned to the pin locations by the BOARD, ASSIGN, and CONNECT modules. The execution of several of the rules results in the modification of the net under scrutiny. Nets which violate any of the rules are considered to be possible design errors, and are flagged to the user. This module is considered to be the "core" of the CAD package.

DOCU - Numerous aspects of the design are sorted and listed in a variety of report formats optimized to present the status of the design in a detailed yet easily referenced manner. Much of the ease of use of the output of the CAD package depends on the proper sorting and presentation of the compiled design information. DOCU is considered to be a "package" because it contains several documentation modules as well as user utility modules.

EC

- Even after a logic design has been completed and fabricated on a wire wrap board and initial design errors have been resolved, later modification may be required, for example, to enhance system capabilities. EC provides a means for making the modification without re-executing the entire ALP procedure. All changes are recorded in such a manner that the designer may track backward through several successive layers of design modification. If any DOCU module is run after the EC is made, the resulting output will indicate the then-current state of the board (i.e., the results of the change will be included).

## DETAILED DESCRIPTION OF INDIVIDUAL MODULES IN THE MAYO ECL CAD PACKAGE

### BOARD

The task of the BOARD module is the creation of an initial "state table" which depends only on the configuration of the wire wrap board being used. The "state table" is a collection of entries describing the current state of the CAD-supported portion of the design process. Since this initial state table depends only on the board configuration, it is only necessary to execute the BOARD module once for a given board configuration if replicates of it are used to fabricate multiboard systems.

The state table entries mentioned above are simply multiple records residing in a large file, with one record for each socket pin on the board. Every record is subdivided into several fields, each representing electrical, mechanical, and topological attributes of the socket pin. Only those fields definable by the BOARD module will be described here; other fields present in the record remain empty (blank or zero) until an appropriate CAD module enters information into them at a later stage of the procedure. Six of the fields in each record associated with a socket pin are related to the board configuration: 1) X coordinate; 2) Y coordinate; 3) Location name; 4) Location pin number; 5) Next available attribute position pointer; and 6) Attribute field.



AD-A097 014

MAYO CLINIC ROCHESTER MINN  
COMPUTER AIDED WIREWRAP INTERCONNECT.(U)  
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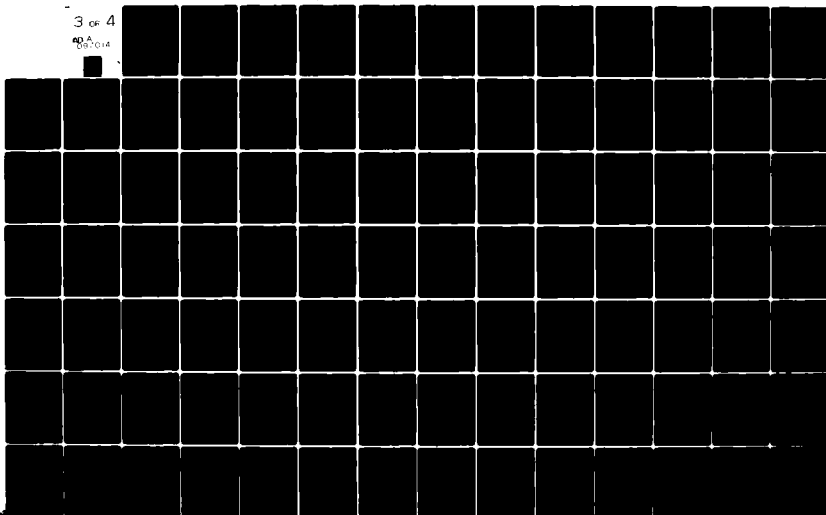
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An hierarchical method is used to concatenate a set of socket pin records iteratively into a large file which defines a logic board. Three levels of description are involved in the iterative procedure: 1) an "element" is defined in terms of attributes; 2) a "row" is defined in terms of elements; and 3) a "board" is defined in terms of rows. This process is schematized in Figure 63.

Each "element" is defined as follows:

```
Element = X, Y, Location Pin Number, Attribute
          X, Y, Location Pin Number, Attribute
          :
```

An element which corresponds to an integrated physical structure, such as a cable connector or a socket for an integrated circuit, may contain any number of pins. The X, Y are the relative coordinates of the pin within the element, while the Location Pin Number assigns a number to the pin as described earlier. The socket board pin may be assigned at most one "board attribute," which is stored in the Attribute field. A socket pin is assigned a board attribute if it is to be connected to the ground plane or to one of the voltage planes when the board is originally fabricated, and is not assigned a board attribute if it is intended to be a signal pin. The entire element is then assigned a name. In Figure 63, E1 and E2 are the element names of a cable connector and an integrated circuit respectively.



MAYO COMPUTER-AIDED DESIGN (CAD) OF  
CIRCUIT BOARD LAYOUT USING  
"ATTRIBUTE/MODULE" TECHNIQUE

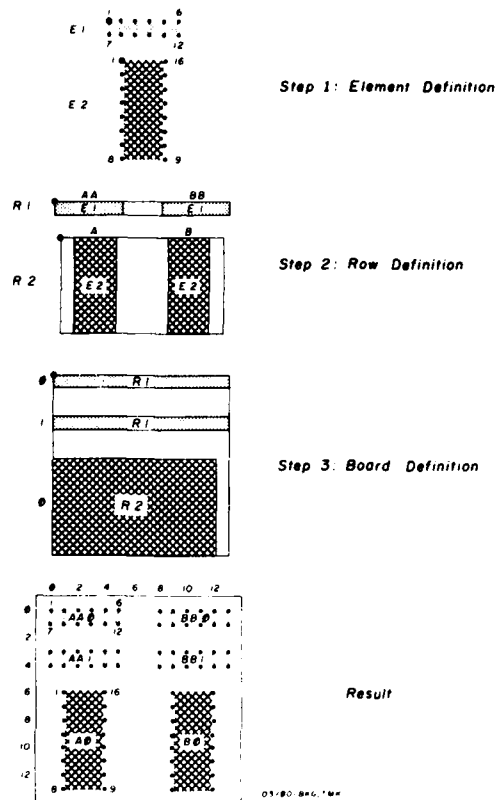


Figure 63

A "row" may be assembled from several elements. Step 2 of Figure 63 depicts the assembly of two rows, named R1 and R2, by the concatenation of elements defined in Step 1. Each row may contain any number and combination of elements. A row is defined as follows:

Row = X, Y, Element Name, First Half of Location Name  
       X, Y, Element Name, First Half of Location Name  
       .  
       .

in which X, Y are the relative coordinates of an element within the row, and the Element Name specifies which of the previously designed elements is to be employed. The first half of the Location Name is assigned an unique set of characters for each element of the row. This is the Board Location Name "column component". Referring to Figure 63, row R1 contains element E1 at Location Name AA and element E1 at Location Name BB, while row R2 contains E2 at Location Name A and E2 at Location Name B.

The final board layout is created from an assembly of previously defined rows, as follows:

```
Board = X, Y, Row Name, Second Half of Location Name
        X, Y, Row Name, Second Half of Location Name
        :
```

in which X, Y are the relative coordinates of the row on the board, Row Name specifies the row to be used, and the characters comprising the Second Half of the Location Name are assigned to the Location Names of each element of the row. This supplies the Board Location Name "row component". In step 3 of Figure 63, the board consists of two copies of R1 and one copy of R2. The row components of the Location Names are shown to the left of the board.

The fully assembled logic board is shown in schematic form at the bottom of Figure 63. The final Location Name for each pin grouping (the groupings coincide with elements) is observed to be the concatenation of the column component and row component. Thus an unique name can be assigned to each pin grouping. The numbers to the left and top of the result represent the X, Y coordinate system, with the origin located at the upper left pin. The numbers associated with groups AAO and AO are the Location Pin Numbers associated with that particular pin grouping, corresponding in this example to connector and chip socket pins, respectively. The input to the BOARD module which produces the result depicted in Figure 63 is shown in Figure 64.

The board design currently used for ECL 100K ceramic dual in-line packages consists of 3 element types and 2 row types and is depicted in Figure 11. The board resembles that of Figure 62 in that there are two sets of groupings: cable connector groupings along one edge, with the rest of the board containing integrated circuit socket pattern groups. The hierarchical approach to board layout and specification saves much effort in comparison to an approach in which each pin is specified. For example, although the ECL 100K DIP board of Figure 11 contains 12,039 socket pins, the entire board is defined by only 154 card images. This obviously compact layout scheme results from the highly repetitive structure of the board.

Element = X, Y, Location Pin Number, Board Attribute

E1 = 0, 0, 1	E2 = 0, 0, 1
1, 0, 2	0, 1, 2
2, 0, 3	0, 2, 3
3, 0, 4	0, 3, 4
4, 0, 5	0, 4, 5
5, 0, 6	0, 5, 6
0, 1, 7	0, 6, 7
1, 1, 8	0, 7, 8, BGND
2, 1, 9	3, 7, 9
3, 1, 10	3, 6, 10
4, 1, 11	3, 5, 11
5, 1, 12	3, 4, 12
	3, 3, 13
	3, 2, 14
	3, 1, 15
	3, 0, 16, BVCC

Row = X, Y, Element Name, First Half of Location Name

R1 = 0, 0, E1, AA	R2 = 1, 0, E2, A
8, 0, E1, BB	9, 0, E2, B

Board = X, Y, Row Name, Second Half of Location Name

BOARD = 0, 0, R1, 0  
0, 3, R1, 1  
0, 6, R2, 0

Figure 64

INPUT TO CREATE THE BOARD LAYOUT  
SHOWN IN FIGURE 63

## COMP

The major function of the COMP module is the conversion of a set of inputs describing the various available part types into a conveniently organized file. This file, referred to as the Component Dictionary, consists of a directory and a large block of data. The COMP module need only be executed when it is desired to modify the dictionary (for example, to add, delete, or update component types).

Each item input to the COMP module consists of a component name (also referred to as part type or part number) for each part type, and the information delineating the physical and electrical characteristics of that component:

Component Name = Pin Number, X, Y, [Component Attributes]  
Pin Number, X, Y, [Component Attributes]

Figure 65 displays three hypothetical component configurations similar to those depicted in a manufacturer's data book. An example of input data to the Component Dictionary for these part types is shown in Figure 66. The Pin Number is a unique number assigned to each pin of the component, while X, Y represents the position of that pin relative to a reference point on the component package (e.g., the upper left corner of the DIP). The measure units represented by X, Y are the same as those used in the BOARD module. The Component Attributes

SPECIFICATION OF ELECTRICAL AND PHYSICAL  
ATTRIBUTES OF LOGIC COMPONENTS FOR  
MAYO COMPUTER-AIDED DESIGN (CAD) PROGRAM

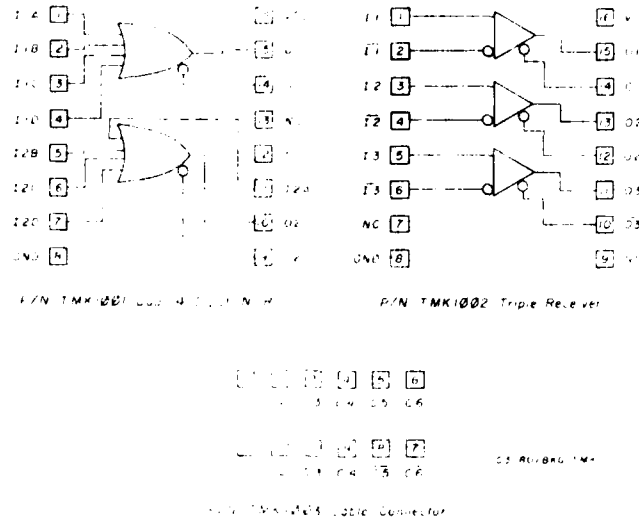


Figure 65

displayed in Figure 66, which represent only a small sample of all possible attribute variations, are described as follows:

- 1) I: Input pin; 2) O: Output pin; 3) GND: Ground pin;
- 4) VCC: Power pin; 5) C: Cable connector pin; and 6) N(K): Signal is the logical complement (NOT) of the signal on pin #K. Attributes 1-5 are referred to as "Simple Attributes," while attribute 6 is defined as a "Linked Attribute" because it links its assigned component pin with another pin on the same component. The exact purpose of each of the possible attributes will be clarified in the section of this report describing the VERIFY module, in Addendum II of Part II of this report, and also in the MAYO CAD User's Guide.

Component Name = Pin Number, X, Y, [Component Attributes]

TMK1001 = 1, 0, 0, I  
 2, 0, 1, I  
 3, 0, 2, I  
 4, 0, 3, I  
 5, 0, 4, I  
 6, 0, 5, I  
 7, 0, 6, I  
 8, 0, 7, GND  
 9, 3, 7, 0, N(10)  
 10, 3, 6, 0, N(9)  
 11, 3, 5, I  
 12, 3, 4  
 13, 3, 3  
 14, 3, 2, 0, N(15)  
 15, 3, 1, 0, N(14)  
 16, 3, 0, VCC

TMK1002 = 1, 0, 0, I, N(2)  
 2, 0, 1, I, N(3)  
 3, 0, 2, I, N(4)  
 4, 0, 3, I, N(5)  
 5, 0, 4, I, N(6)  
 6, 0, 5, I, N(7)  
 7, 0, 6  
 8, 0, 7, GND  
 9, 3, 7,  
 10, 3, 6, 0, N(11)  
 11, 3, 5, 0, N(10)  
 12, 3, 4, 0, N(9)  
 13, 3, 3, 0, N(8)  
 14, 3, 2, 0  
 15, 3, 1, 0  
 16, 3, 0, VCC

TMK1003 = 1, 3, 1, 1, C, N(12)  
 2, 1, 1, C, N(11)  
 3, 2, 0, C, N(10)  
 4, 3, 0, C, N(9)  
 5, 4, 0, C, N(8)  
 6, 5, 0, C, N(7)  
 7, 5, 1, C, N(6)  
 8, 4, 1, C, N(5)  
 9, 3, 1, C, N(4)  
 10, 2, 1, C, N(3)  
 11, 1, 1, C, N(2)  
 12, 0, 1, C, N(1)

Figure 66

COMPONENT DICTIONARY INPUT

The example of Figures 65 and 66 omits one important feature of the COMP software. The full designation of an ECL 100K part type is comprised of six decimal digits and a two letter suffix, for example, 100102DC. The first letter may be (at present) a D, indicating a dual in-line package; F, indicating a flat pack; or L, indicating a leadless chip carrier. The second letter may be (at present) a C, indicating ceramic packaging; or a P, indicating plastic encapsulation. The COMP module permits encoding of the entire component designation, and recognizes that the physical and electrical characteristics of a given part type packaged in different encapsulations will display, for example, different thermal and propagation delay characteristics. The COMP module thus distinguishes between, for example, 100102DC, 100102DP, 100102FC, and 100102LC, and provides for the incorporation of the appropriate device parameters into the component library for use by later modules described below.



## NET

The previous two sections, BOARD and COMP, have described modules that need not be invoked frequently. For example, once a board configuration has been developed, the BOARD module is not required again until a new style of logic panel is designed. COMP is needed for only one run when all of the component types available to the designer are known and have been described. The information which does change for each logic design is that specifying placement of individual integrated circuits on the logic board, and the topology of their interconnections. The order in which the operations of placement and interconnection are performed is completely arbitrary, as it is desirable to allow the logic design to be performed without regard to the final physical placement of components. Physical placement of components can be optimized to the given design after the electrical portion of the engineering design effort has been completed.

The input data for the net module represents topological interconnect information, which is independent of component placement; this data is then processed and stored for later use when the physical interconnect and layout is performed. In the following discussion, the term "node" refers to a component pin, while a "net" is a collection of nodes. The operations performed by the NET module include 1) input of topologic data describing each node; 2) input of topologic

connected to the other nodes. The nodes are numbered 1 through 10. The nodes are connected to each other by lines. The nodes are numbered 1 through 10. The nodes are connected to each other by lines. The nodes are numbered 1 through 10. The nodes are connected to each other by lines.

The following information is required for each node: 1) Net Name; 2) Volume 1; 3) Page 1; 4) Component Number; 5) Component Pin Number; 6) Signal Flow Attribute; 7) Signal Flow Attribute (optional). The usual preparation method of specification for the CAD program is the encoding; and entering into the text file of all of the nodes in a given case according to the order is desired. For example, in Figure 67, the nodes are numbered 1 through 10. The nodes are connected to each other by lines. The nodes are numbered 1 through 10. The nodes are connected to each other by lines.

The following information is required for each node: 1) Net Name; 2) Volume 1; 3) Page 1; 4) Component Number; 5) Component Pin Number; 6) Signal Flow Attribute; 7) Signal Flow Attribute (optional). The usual preparation method of specification for the CAD program is the encoding; and entering into the text file of all of the nodes in a given case according to the order is desired. For example, in Figure 67, the nodes are numbered 1 through 10. The nodes are connected to each other by lines. The nodes are numbered 1 through 10. The nodes are connected to each other by lines.

- 12 -

actually node attributes) are encoded as "S" for a signal source and "D" for a signal destination. In this example, a group of signals are introduced into the board through Connector #1 and are extracted from the board through Connector #2. There are no Net Attributes in this example. Refer to the ECL CAD package User's Guide for additional information.

The Net Cross Reference Listing is a useful output data format, or "report", intended to assist the engineer in design debugging and node input verification, particularly during the early phases of a new system design. This hard-copy output presents in a single printed block the sources and then the destinations for each net, and also lists the vellum print page coordinate of each node, thereby simplifying the task of tracing through a net. Although not shown by the example of Figure 67, very frequently several portions of a single net are scattered among multiple vellum sheets, greatly complicating the design task. In such cases, a concise map and cross reference listing is extremely useful if alterations in all nodes of a net are required.

<u>Net</u> <u>Name</u>	<u>Print</u> <u>Page/Coordinate</u>	<u>Component #</u>	<u>Pin #</u>	<u>Signal</u> <u>Flow</u>
DATA1	01A1	1	1	S
DATA1C	01A1	1	12	S
DATA2	01A1	1	2	S
DATA2C	01A1	1	11	S
DATA1	01A1	3	1	D
DATA1C	01A1	3	2	D
DATA2	01A1	3	3	D
DATA2C	01A1	3	4	D
BIT1	01A1	3	15	S
BIT2	01A1	3	13	S
DATA3	01A2	1	3	S
DATA3C	01A2	1	10	S
DATA3	01A2	3	5	D
DATA3C	01A2	3	6	D
BIT3	01A2	3	11	S
BIT1	01B1	4	1	D
BIT2	01B1	4	2	D
BIT1	01B1	4	5	D
SIG1	01B1	4	15	S
SIG1	01B1	4	6	D
BIT3	01B1	4	7	D
SIG2	01B1	4	10	S
SIG2C	01B1	4	9	S
SIG2	01B1	2	1	D
SIG2C	01B1	2	12	D

Figure 68  
NET INPUT FOR CIRCUIT SHOWN IN FIGURE 67

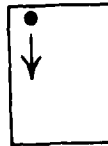
## ASSIGN

When a logic design has been fully analyzed by the user and all components of the design have been entered, the components are assigned to a board. This is done on one or more boards. This function is presently implemented in the ELL 100A CAD package and is not automated. For example, the selection of a specific type of PCB carrier, the rack and slot location assignment on the boards is not automated, and the PCB components are automatically positioned to minimize wire length such as connection length. At present, these optimization tasks must be carried out by the designer. When these functions will be automated in the near future, the present CAD software has been configured to collect statistics concerning the placement and usage of these components which in turn will be employed for further refinement of the entire CAD package.

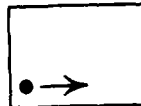
The ASSIGN module must be supplied with the following input data: 1) Component Numbers; 2) Board Location Names; 3) Board Location Pin Numbers; 4) Component Names; and 5) Component Orientations. It is at this stage of the CAD procedure that the Component Number is linked to a Board Location. The Board Location Name and Pin Numbers allow the component to be mapped onto a set of physical board coordinates. The Component Name specifies the part type to be retrieved from the Component Dictionary for placement onto the logic board, with the reference

pin on the component (coordinate 0,0) placed at the prespecified position on the board. All other pins on that component are in turn positioned with respect to this reference pin (a component need not actually have a physical pin at the 0,0 coordinate; however, all pins are treated as if a pin actually exists at that location). The Component Orientation specifies four possible orientations of the component with respect to the reference pin, i.e., down (default); right; up; or left (as depicted in Figure 69).

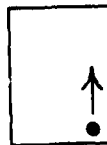
The assignment process modifies the state table created by the BOARD module. The record fields modified by this module include: 1) Component Numbers; 2) Component Pin Numbers; 3) Component Names; 4) Next Available Attribute Pointers; and 5) Attributes. A copy of the state table produced by the BOARD module is prepared for use by the ASSIGN module. If a component contains N pins, then a single assignment statement causes the modification of N records in the state table. The first three fields described above are self explanatory. The attribute field, which is of variable length, may or may not contain attributes inserted by the BOARD module. This field is updated with attributes associated with the particular component pin being assigned (however, the pin may have no attributes). The attribute pointer is updated to reflect the modification.



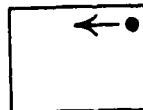
*Down (Default)*



*Right*



*Up*



*Left*

## COMPONENT PLACEMENT ORIENTATIONS

*Figure 69*



## CONNECT

After all components in a system under design have been assigned to specific locations on the logic board, the net nodes can be connected together by entering links into the records of the state table. To prevent wavefront reflections from unterminated transmission line stubs, the net nodes are restricted by the ECL wiring protocols described in Part I to a chain connection (i.e., the CAD program permits at most one predecessor and at most one successor for a given node). After the nodes have been linked, any given node in the net may be accessed, a path may be threaded through the links to the initial node (which is almost always a source), and the entire net may then be traversed from source to termination.

Prior to the execution of the CONNECT module, a special file is prepared by the NET module which defines each net in terms of its name and the set of attributes [(Component Number i; Pin Number i)] comprising all nodes in the net. The CONNECT module reads the contents of the set and then performs the mapping operation:

$$(\text{Component Number } i, \text{ Pin Number } i) \longrightarrow (X_i, Y_i)$$

by utilizing the information in the state table prepared by the ASSIGN module. The set of geometrical coordinates produced by this procedure is used to optimize the physical topology of the

interconnects. The optimizer, a traveling salesman algorithm, generates an ordered sequence of the nodes in which all of the signal sources are grouped together, and all destination nodes are grouped together (as specified by the design rules for subnanosecond ECL); finally, the traveling salesman algorithm interconnects the nodes in such a manner that the sum of the interconnect lengths for each string is near minimum.

The state table record fields modified by the CONNECT module are: 1) Net Names; 2) Predecessor Pointers; and 3) Successor Pointers. These modifications are carried out on every node of a given net. The Net Name not only associates a specific node with a specific net, but also identifies whether or not a node has been assigned to any existing net (by the presence or absence of a name), thereby allowing a later software module to establish a list of unused pins. The ordering imposed by the optimizer produces an initial node, a linear chain of interconnected intermediate nodes, and a final node. The Net Name and record number for the initial node are stored in a specially reserved file which serves as a list of entry points to allow entry into the state table given only the Net Name. The initial node is assigned a predecessor pointer value of zero, while the successor pointer contains the record number of the next node in the string. This construct is propagated through all successive nodes in the string until the terminal node is reached, which is assigned a successor pointer value of zero.

## VERIFY

The VERIFY module checks the logical design and physical layout design to assure that all of the ECL design rules are followed; this software module also supplies terminations and enforces the appropriate transmission protocols. At its current level of sophistication, the verification module is not capable of identifying functional design errors, e.g., via simulation of the logical operation of the system, or physical errors, e.g., via timing analysis. It is our intent, however, to evolve these additional capabilities in future work, which can easily be implemented through software modules operating on the state table. The primary procedure executed by this module is termed Design Rule Checking, which identifies whether or not a design conforms to a set of design rule protocols. The adherence of the design to these restrictions generally decreases system checkout time and improves reliability and maintainability of the operational system. During the course of invoking the ECL design protocols, the CAD actually performs a portion of the design through its assignment of terminators and selection of wiring protocols.

The categories of verification performed are: 1) net validation; 2) assessment of net loading; and 3) selection of wiring protocols and assignment of terminators. A partial list of verifications used in the current version of the ECL 100K CAD is presented in Addendum II, Part II, of this report.

Testing for design errors occurs during the net validation procedure. Net loading assessments apply a variety of fanout restrictions, which vary considerably between 1) logic HIGH nets used for establishing fixed levels on the inputs of components; 2) signal nets; and 3) clock drive nets. The software responsible for the assignment of wiring protocols and terminations selects the correct terminator resistors and wiring schemas for the nets as a function of net type and internode run length.

The first task performed by the VERIFY module is the retrieval of terminator resistor locations and ground pin locations from the state table, information which is required to perform automatic termination and transmission protocol implementation. Then each net (i.e., each set of node records) is retrieved from the file by an indirect access through the Initial Node Table produced by the CONNECT module; next, the net validity rules are applied; net loading rules are invoked; and finally, terminations and transmission protocols are established. If any of the design rules is found to be in violation, a diagnostic message is output and the next rule is applied. By continuing to invoke successive rules even after an error has been identified in a string, a maximum number of diagnostic steps can be executed before halting the procedure for the given net. However, termination and transmission protocols are not applied if a design rule has been violated.

The results of the termination and transmission protocol application are employed in the modification of the state table. A termination resistor assigned to any given net must be included in the net by a topologic linkage, and the net name must be assigned to the newly connected pin. If the twisted pair transmission protocol is used, a new net is created, i.e., the (ground) wires which are twisted with the signal wires. All of these nodes are then labeled to reflect the fact that they are members of a special type of net, i.e., a "ground net", which is linked to the signal net to which it is physically related.

The result of a successful run of VERIFY (i.e., successful in that no rules were found to be in violation, all nets were properly terminated, and transmission schemes were correctly implemented) is a completed state table and the updated set of net names. This is the goal of the "design phase" which includes the execution of the BOARD, COMP, NET, ASSIGN, CONNECT, and VERIFY software modules. The completed state table is then employed by other modules executed at a later time in the overall procedure to produce the required documentation reflecting the design state of the board (see the following description of the DOCU and EC modules).

## DOCU

DOCU is a collection of software modules which are executed selectively at various stages of the design process. The overall task of this set of routines is the creation of displays of selected information reflecting the state of the system design, to serve either as an aid in design refinement, or as the final design documentation. A critical feature of the output displays is the ordering of the information and the specialization of their formats to allow easy access to and cross reference of the design data base by the designer. The modules rely heavily on a sorting routine to produce the desired ordering of the output material.

The documentation routines are divided into two groups:

- 1) those which can be executed as "batch" jobs; and 2) those which must be operator-interactive and executed from a display screen terminal device. The major batch jobs perform the following functions:

- 1) Printing of the entire state table;
- 2) Printing of the state table records for a given Location Name;
- 3) Printing of a variety of miscellaneous files;
- 4) Output of the component dictionary listing;
- 5) Printing of the net cross-reference listing;
- 6) Printing of state table records for all nodes in a given net;
- 7) Listing of component assignments; and
- 8) Printing of all material in a "Final Documentation" format.

The Final Documentation module is generally executed only after a given design is completely verified, because it generates output information in a format specifically intended for the preparation and fabrication of the actual logic board. Examples of the information printed include: 1) all committed board locations; 2) unused board locations; 3) unused sections in multi-section chips; 4) a map of committed and uncommitted pins on each integrated circuit; 5) uncommitted terminator pack pins; 6) power requirements for the entire logic board; 7) a component placement map; 8) special instructions for preparation of a logic panel prior to wiring (e.g., pins requiring special spot-facing); 9) wirelist printouts to be used by the wire wrap technician or by an automated wire wrap machine.

Several of the operator-interactive software modules presently available include: 1) displays of the state table record for a given board location; 2) displays of all nodes in a given net; 3) displays of assigned component inputs associated with a given output, or of all outputs associated with a given input.

## EC

After a logic panel has been designed and fabricated, in a system prototyping environment it is frequently necessary to make changes (referred to as Engineering Changes), either to correct a design error or to install a design enhancement. Since it would be clearly undesirable to re-execute the entire CAD package for these usually minor changes, a specialized "EC" module has been developed for this task which allows an entry into the current state table and the execution of a selected subset of modifications in a controlled manner. A minimal set of four capabilities is required, including: 1) addition of a component; 2) deletion of a component; 3) interconnection of two pins; and 4) disconnection of two pins.

The EC module is an operator-interactive program executed from a screen terminal. All commands executed through this software routine are documented in such a manner that they may be backtracked at a later date. Each of the four functions described above requires the performance of a large number of operations on the state table. However, during a given update, the state table remains unchanged until all of these operations are carried out successfully, thereby preventing an erroneous command from destroying any of the records established previously (and correctly) in the state table.



The addition or deletion of a component results in the modification of one record for every corresponding pin of the component. Only those characteristics related to the specific component, e.g., component type, component number, pin number, and component attributes are modified. Board or net characteristics must remain untouched. The connection or disconnection of two pins changes only the net characteristics of the pin. Information concerning the type of connection/disconnection (i.e., single rail, twisted pair with ground, or differential twisted pair) is retrieved from appropriate files as required to perform these modifications.

## Operational Test of the EDA-12 Package in a System Design Environment

To increase the utility of the completed CAD package in an engineering design environment, and to aid in the detection of software errors in the CAD, a development, an actual hardware design was required as a reference. The dual logic board system of the Third Demo, a Single Demonstration Test Circuit served this function, with transfer of portions of the engineering data from this design to the CAD, then executed, and the CAD output compared with manually prepared layouts and validation data. Numerous errors in both the CAD and the engineering data were detected in this manner, thereby improving both. This process was continued throughout the entire design effort of the Third Demonstration Test Circuit; examples of input and output drawings from the CAD package for this system design are among the deliverables from the Year One effort.

The addition or deletion of a component results in the modification of one record for every corresponding pin of the component. Only those characteristics related to the specific component, e.g., component type, component number, pin number, and component attributes are modified. Board or net characteristics must remain untouched. The connection or disconnection of two pins changes only the net characteristics of the pin. Information concerning the type of connection/disconnection (i.e., single rail, twisted pair with ground, or differential twisted pair) is retrieved from appropriate files as required to perform these modifications.

## ADDENDUM I - 11.7.77

### STATE TABLE SAMPLE FOR EXAMPLE DISCUSSED IN TEXT

The following three tables describe the state table records corresponding to board location for the example circuit discussed in the text. The state table is displayed after it has been created by the BOARD module (Figure 70), after components have been assigned by the ASSIGN module (Figure 71), and after the net interconnections have been processed by the CONNECT module (Figure 72). The final system design state displayed in these tables represents the data which would be made available to the VERIFY module for design rule verification.

The information displayed in the following tables has the following definitions:

LOC:	Board Location Name. Pin Number
X, Y:	Board Coordinates
CMP#:	Component Number
TYPE:	Component Type
PIN:	Component Pin Number
NET:	Net Name
PREV:	Previous node in net (- = none)
NEXT:	Next node in net (- = none)
ATTRIBUTES:	Set of Attributes presently assigned

LOC	X, Y	CMP#	TYPE	PIN	NET	PREV	NEXT	ATTRIBUTE
A0.01	1,6							
A0.02	1,7							
A0.03	1,8							
A0.04	1,9							
A0.05	1,10							
A0.06	1,11							
A0.07	1,12							
A0.08	1,13							BGND
A0.09	4,13							
A0.10	4,12							
A0.11	4,11							
A0.12	4,10							
A0.13	4,9							
A0.14	4,8							
A0.15	4,7							
A0.16	4,6							BVCC

Figure 70

RESULT OF EXECUTION OF THE BOARD MODULE

LOC	X, Y	CMP#	TYPE	PIN	NET	PREV	NEXT	ATTRIBUTES
A0.01	1,6	3	TMK1002	01				I, N(1,7)
A0.02	1,7	3	TMK1002	02				I, N(1,6)
A0.03	1,8	3	TMK1002	03				I, N(1,9)
A0.04	1,9	3	TMK1002	04				I, N(1,8)
A0.05	1,10	3	TMK1002	05				I, N(1,11)
A0.06	1,11	3	TMK1002	06				I, N(1,10)
A0.07	1,12	3	TMK1002	07				
A0.08	1,13	3	TMK1002	08				BGND, GND
A0.09	4,13	3	TMK1002	09				
A0.10	4,12	3	TMK1002	10				O, N(4,11)
A0.11	4,11	3	TMK1002	11				O, N(4,12)
A0.12	4,10	3	TMK1002	12				O, N(4,9)
A0.13	4,9	3	TMK1002	13				O, N(4,10)
A0.14	4,8	3	TMK1002	14				O, N(4,7)
A0.15	4,7	3	TMK1002	15				O, N(4,8)
A0.16	4,6	3	TMK1002	16				BVCC, VCC

Figure 71

RESULT OF EXECUTION OF THE ASSIGN MODULE

CON	X, Y	CHIP	TYPE	PIN	NET	PREV	NEXT	ATTRIBUTES
A0.01	1, 6	3	TMK1002	01	DATA1	0, 0	--	I, N(1, 7), D
A0.02	1, 7	3	TMK1002	02	DATA1C	0, 1	--	I, N(1, 6), D
A0.03	1, 8	3	TMK1002	03	DATA2	1, 0	--	I, N(1, 9), D
A0.04	1, 9	3	TMK1002	04	DATA2C	1, 1	--	I, N(1, 8), D
A0.05	1, 10	3	TMK1002	05	DATA3	2, 0	--	I, N(1, 11), D
A0.06	1, 11	3	TMK1002	06	DATA3C	2, 1	--	I, N(1, 10), D
A0.07	1, 12	3	TMK1002	07				
A0.08	1, 13	3	TMK1002	08				BGND, GND
A0.09	4, 13	3	TMK1002	09				
A0.10	4, 12	3	TMK1002	10				O, N(4, 11)
A0.11	4, 11	3	TMK1002	11	BIT3	--	9, 12	O, N(4, 12), S
A0.12	4, 10	3	TMK1002	12				O, N(4, 9)
A0.13	4, 9	3	TMK1002	13	BIT2	--	9, 7	O, N(4, 10), S
A0.14	4, 8	3	TMK1002	14				O, N(4, 7)
A0.15	4, 7	3	TMK1002	15	BIT1	--	9, 6	O, N(4, 8), S
A0.16	1, 6	3	TMK1002	16				BVCC, VCC

Figure 72

RESULT OF EXECUTION OF THE CONNECT MODULE

## ADDENDUM II TO PART II

### PARTIAL SUMMARY OF DESIGN RULE TESTS

#### NET VALIDATION (Partial List)

- 1) At least one source in each net.
- 2) At least one destination in each net.
- 3) If a small scale integrated (SSI) gate output pin is committed, at least one input pin must also be committed (except for logic HIGH biasing nets).
- 4) Flip flops and registers with at least one committed output must have at least one clock input and/or set and reset inputs committed.
- 5) If any gate, flip-flop, or other component possesses both true and complement outputs, and one of these outputs is used in the logical design as the source in a signal string, but the other output is unused in the logical design, the CAD must nonetheless create a shunt termination string for the otherwise unused output. This approach assures that AC return path currents on the logic boards will be minimized.
- 6) If a cable connector destination node is included in a net, there must be only one source node; the source's signal complement node must drive the paired cable connector node.



- 7) If a cable connector source node is in the net, there must be only one destination node; the destination's signal complement node must receive from the paired cable connector node.
- 8) Clock signals transmitted through a multiconductor cable must occupy one of the two edge pairs in the cable; the immediately adjacent conductor pair should be grounded on both ends of the cable.
- 9) A mechanical switch (e.g., a DIP switch) is only allowed in a logic HIGH net.

#### NET LOADING (Partial List)

- 1) A driving gate used to generate a DC logic HIGH should not drive more than ten loads.
- 2) A signal net should not contain more than six loads.
- 3) A clock net should not contain more than four loads of the system clock frequency is greater than 50 MHz, and not more than seven loads if the system clock is less than 50 MHz.

#### INTERCONNECTION PROTOCOLS (Partial List)

- 1) If a gate, flip flop, or register has paired outputs available and only one is committed by the design, the other must be assigned a termination.
- 2) The most frequently employed protocol will be shunt termination single-rail.

- 3) The next most frequently employed protocol will be differential, primarily for offboard signals, and secondarily for long on-board clock runs.
- 4) A single-rail internode run less than 1 inch in length may be via a single wire untwisted with ground.
- 5) All single-rail runs longer than 1 inch should be twisted with ground.
- 6) All signal wires longer than 20 cm should be considered for assembly with wire wrappable coax.

### PART III

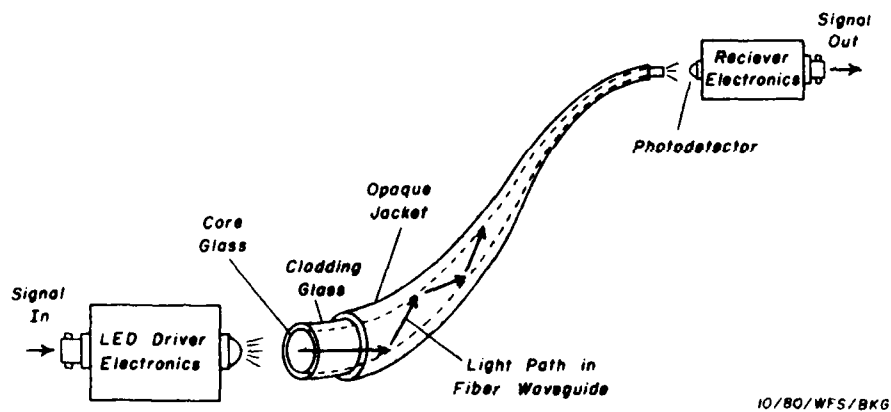
#### OPTICAL COMMUNICATION SYSTEMS--AN OVERVIEW

The extensive examination of interboard communications protocols carried out for this project, and described in Part I, Section 6 of this report, delineated a number of weaknesses in these electrically based transmission approaches which render them sensitive to local and global electrical and mechanical background conditions. Contaminants such as intercable cross-talk, common mode noise from the global environment, reflections, and standing waves all degrade the ability of these electrically based communications protocols to transmit word-wide data in a reliable manner, particularly at very high system clock rates. In an attempt to identify alternate approaches to high bandwidth communication between the subchasses of a high-speed processor, we have investigated the possibility that optical communications pathways based upon the emerging fiber optics technology might provide a suitable alternative to conventional copper wire approaches. The following material was prepared in the course of a review of the fiber optics technology at its present level of development.

As depicted in Figure 73, an optical communication system, or fiber optic link, converts an electronic signal to its light analog (wavelength  $\lambda = 0.8 \mu\text{m}$  to  $1.55 \mu\text{m}$ ) by means of either a

Light Emitting Diode (LED) or an Injection Laser Diode (ILD). This light or optical signal is coupled into one end of a glass fiber which has an outer shell, or cladding, of a lower refractive index than its core. After propagating along the axis of the fiber, the optical signal is directed at the surface of a photo detector (a PIN or APD diode) at the opposite end of the fiber, which converts the optical signal back to an electronic signal (Reference 7).

#### BASIC FIBER OPTICS COMMUNICATION LINK



- Fiber Fused Silica or Glass Composition
- Source 0.8 to 1.06  $\mu\text{m}$  LEDs or Laser Diodes
- Detector Silicon PIN or Avalanche Photodiode

From L. Bergstein, GWU/Wash. D.C., "Fiber Optic Communications", Feb. 1979

Figure 73

## History

The first rigorous demonstration that light can be guided through a curved transparent medium such as water flowing from a hole in the side of a tank was accomplished by John Tyndall in 1870. By 1880, Alexander Graham Bell had studied the possibility of transmitting speech on a beam of light via a device he called a "photophone." Seventy years thereafter flexible viewing devices called fiber bronchoscopes were developed, and are now commonly used in a variety of medical diagnostic procedures. However, the most important advance of the 1950s was the development by N. S. Kapany of a technique for manufacturing continuous glass fibers which were themselves coated with a second layer of glass with chemical and optical properties different from the main core of the fiber. In 1967, researchers in England proposed that this "fiber optic" could form the basis of a new communication system; however, attenuation factors of 1000 dB/km were quite common for fibers manufactured at that time. In 1970 Corning Glass announced the development of fiber optics materials with attenuation factors of less than 20 dB/km. This breakthrough created a growing perception that fiber optics for communications systems might become realistic within a reasonable duration (Reference 8). It is now possible to obtain modestly priced off-the-shelf fibers with attenuation factors of from 2 to 6 dB/km.

## Advantages of the Fiber Optic Communication Systems

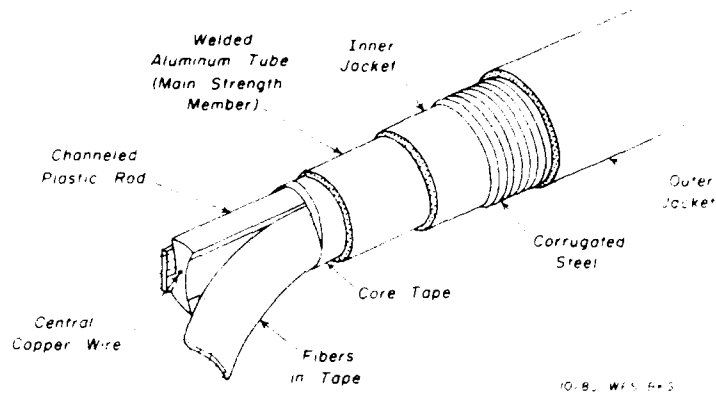
There are many reasons to consider fiber optics for communication systems as replacements for coaxial or twisted pair cables: 1) Considerable savings in size and weight may be achieved, as one fiber optic filament several mils in diameter can replace a multiconductor copper cable several inches in diameter. 2) Optical transmission is immune to ambient electrical noise, ringing, and electromagnetic interference, and is not a generator of electrical noise. 3) Fiber optic communication systems are relatively immune to crosstalk generated by adjacent fibers in a large bundle or cable. 4) Optical cables may be used safely in explosive environments. 5) Properly designed optical transmission lines and couplers are relatively immune to adverse temperature and moisture conditions, and can even be used for underwater cable. The coated fibers themselves are immune to thermal damage at temperatures up to 1000°C, whereas coax cable is limited to approximately 300°C extremes. 6) The required spacing of repeaters in a long transmission path employing low attenuation fiber optic cable is greater than for conventional wire cable systems. 7) Even at the present state of the art, the costs of fiber optic cables are approximately the same as, or less than, premium grade coaxial cable, and will soon become much less expensive as fiber optic cable production is increased. 8) The information carrying capacity of most optical communication

systems utilizing modern low loss fiber optic cables can be upgraded by simply upgrading the optical source from a light emitting diode (LED) to an injection laser (see explanations below). 9) In general, the installation costs of fiber optic cables are lower than for metal cables. 10) Fiber optics links conserve resources since they utilize abundantly available silicon-based materials rather than copper.

Fiber optic systems are beginning to find wide application in almost every facet of communications: 1) power transmission line protection and control systems; 2) power plant supervisory and control systems; 3) highway, airport and railway communication and traffic control/supervisory systems; 4) industrial plant communication control/supervisory systems; 5) laboratory automatic systems; 6) computer networks and links; 7) medical information and diagnostic support systems; 8) telephone and video communication systems.

The general characteristics of fiber optic cable are shown in Figure 74, displaying a heavy duty cable for telephone systems which can be installed by regular crews; Figure 75 depicts a similar cable exhibiting slightly different construction. The fibers are secured around a central strength member and then wrapped with tape, plastics, metal tubes and plastic jackets. Cable characteristics such as strength and cost are presented in Figure 76; a comparison of fiber optic cables with metallic cables is exhibited in Figure 77.

CONSTRUCTION OF FIBER OPTIC CABLE MANUFACTURED  
BY GENERAL CABLE COMPANY

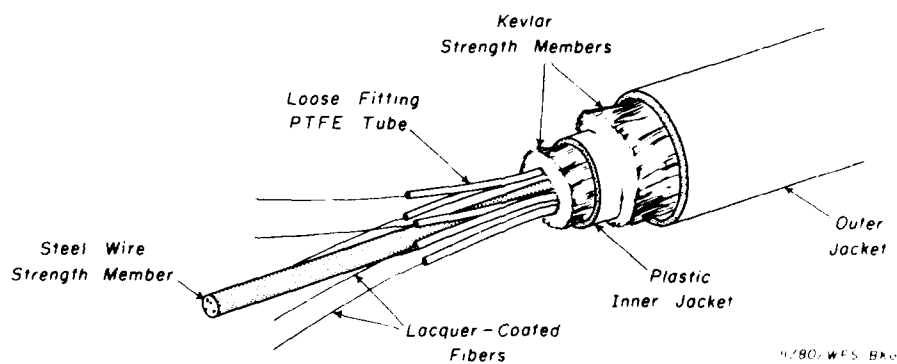


EXTERNAL CONSTRUCTION FOLLOWS TRADITIONAL TELEPHONE CABLE PRINCIPLES  
HEAVY DUTY CABLE WHICH CAN BE INSTALLED BY REGULAR CREWS

From: R. G. B. (U.S. Patent 3,111,111) Filed: 1964, 1965, 1966, 1967, 1968, 1969

Figure 74

CONSTRUCTION OF FIBER OPTIC CABLE MANUFACTURED  
BY SIECOR COMPANY



Minimum Stress on Fiber in Cable Manufacture Results in Superior  
Optical Performance

From: C. Bergstein, GWU (Wash. D.C.), Fiber Opt. Communications, Feb. 1970

Figure 75

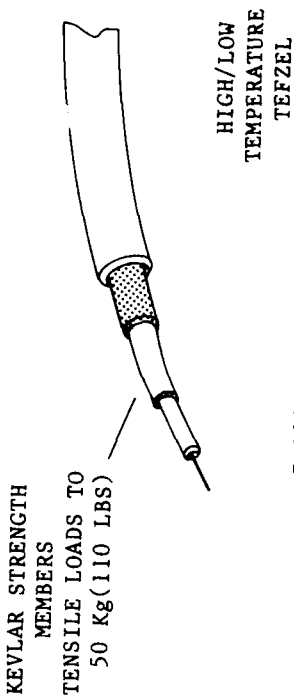


# CABLE CHARACTERISTICS

## CONFIGURATION

### SINGLE FIBERS

### BUNDLE FIBERS



NO FIBERS:

PULL STRENGTH:

BEND RADIUS:

CABLE

FIBER

CABLE DIA:

WEIGHT:

TESTING ALL TYPES):

6-19  
400 LB

5 CM  
.5 CM  
5.5 MM  
30 KG/KM

6-8  
400 LB

5 CM  
.5 CM  
5.5 MM  
30 KG/KM

CRUSH  
ABRASION  
IMPACT  
ENVIRONMENTAL

FIBERS:

STEP INDEX

GRADED INDEX

PLASTIC CLAD

SILICA

6-20 dB/KM @ 30 NSEC-KM  
6-20 dB/KM @ 2.5 NSEC-KM

40 dB/KM @ 50 NSEC-KM

APPROX COST:

1978

1980

(6 FIBER)  
\$8.00/METER  
\$3.00/METER

(6 FIBER)  
\$8.00/METER  
\$3.00/METER

100 to 700 dB/KM @ 250 NSEC-KM

40 dB/Km @ 50 NSEC-KM

\$4.00/METER  
\$2.00/METER

From: L. Bergstein, GWU (Wash. D.C.), "Fiber Optical Communications", Feb. 1979

Figure 76

	<u>Fiber Optics</u>	<u>Coax</u>	<u>Twisted Pair</u>
Dielectric Isolation:	Yes	No	No
Interference Immunity:	Immune	Limited	Limited
RFI/EMI -			
Ground Currents -	None	Poor	Poor
Crosstalk Performance -	Excellent	Limited	Poor
EMP Hardness	Immune	Very Poor	Very Poor
Nuclear Hard:	Moderate	Yes	Yes
Bandwidth:	>1GHz/1000 ft	≤ 200MHz/1000 ft	≤ 1MHz/1000 ft
Attenuation:	2 to 400 dB/km	Freq dependent	Freq dependent
Withstanding Temperature	1000° C	≤ 300° C	≤ 300° C
Operating:	-55° C to +155° C	-55° C to +80° C	-65° C to +200° C
Bend Radius:	Good	Poor for larger cables	Good
	.25 - 2 inch	1 inch	1/2 inch
Strength:			
Fiber	300,000 psi	≤ 70 psi (CU)	≤ 70 psi (CU)
Cable	100-600 lb	29 lb	25 lb
Salt and Humidity:	Stress Corrosion	Corrosive	Corrosive
Sparks/Fire Hazard:	No	Yes	Yes
Shorts/Loading Failures:	No	Yes	Yes
Lightweight Materials:	Yes	No	No
	(65 lb/km for rugged cable)	95 lb/km	82 lb/km
Cable Costs (1978):	\$0.10 ft to \$4 ft	\$0.05 ft	\$.05 to .20 ft
Interface Electronics:			
(Component Costs Only)			
Complexity -	Low to high	Low to moderate	Low
	\$10 to \$500	\$1 to \$20	\$1

From: L. Bergstein, GWU (Wash. D.C.), "Fiber Optical Communications", Feb. 1979

Figure 77

COMPARISON BETWEEN FIBER OPTIC AND METALLIC CABLE

## Optical Waveguide

There are two general types of optical fibers used for purposes of communication: multimode and single mode (Figure 78). A multimode fiber is one designed to transmit light containing a broad range of spectral components or modes, whereas single mode fibers are designed to transmit light of a single frequency. Note that there are two types of multimode fibers, namely, step index and graded index (note the "index profile" in Figure 78). The step index fiber is characterized by a relatively large diameter core exhibiting a uniform index of refraction; however, the index of refraction of the outer glass coating, or cladding, abruptly becomes lower than that of the core. This step change in refractive index causes light entering the fiber at all angles greater than a so-called "critical angle" to be reflected from the inner surface of the cladding back into the core of the fiber, preventing escape of light photons through the surface of the fiber. Consequently very efficient, low loss light propagation down the length of the fiber may be demonstrated. Such fibers are easy to manufacture, and may be used with light emitting diode sources in relatively low or moderate bit rate applications (note the depicted pulse shape degradation under "pulse in" and "pulse out" Figure 78) (References 7,9,10).

The second type of multimode fiber is the "graded index" structure, characterized by an index of refraction which becomes

# REFRACTION INDEX PROFILES AND FREQUENCY RESPONSES OF FIBER TYPES

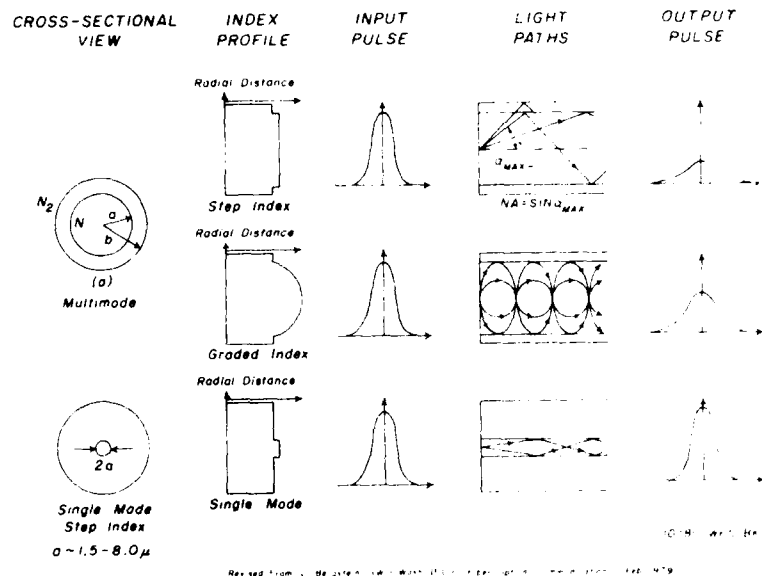


Figure 78

progressively lower from the central axis of the core to the cladding (see "index profile," Figure 78). This causes the higher light modes propagating through the fiber to experience a phase shift as they move from the center of the fiber toward the cladding, bending them back towards the center of the fiber. Fibers manufactured in this manner exhibit a wider bandwidth frequency response than the step index fibers, and, as depicted in Figure 78, by a higher amplitude output pulse relative to the step index output pulse (References 7,9,11). The multimode

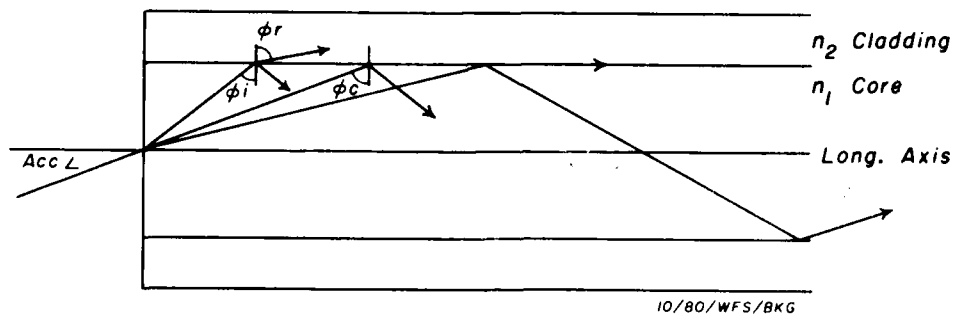
fibers are characterized (Figure 78) by a core of radius "a," which is less than the radius "b" of the entire cladded fiber but much greater than the wavelength of light transmitted through the fiber. The radius "a" of the core is usually in the range of 25 to 150  $\mu$ m. The index of refraction of the cladding,  $N_2$ , is less than that of the core,  $N_1$ , with a difference between the two of about 0.1.

An optical system inherently possessing higher frequency response (note the high amplitude "output pulse" depicted in Figure 78) than either of the multimode fibers is the single mode system. The small diameter of the core of such a fiber, approximately 3 to 16 microns, and its reliance upon light of a single wavelength mandates a light source with a narrow spectral width; single mode fibers thus almost always require a laser light source (Reference 11).

#### Ray Propagation in a Dielectric Multimode Waveguide

As depicted in Figures 79 and 80, ray propagation in a multimode waveguide consists of meridional rays which pass through the waveguide longitudinal axis, and skew rays which do not. For meridional ray propagation consider the dielectric boundary between the core and the cladding (Figure 79).

# MERIDIANAL RAY PROPAGATION IN MULTIMODE DIELECTRIC WAVEGUIDE



From: L. Bergstein, GWU (Wash. D.C.), "Fiber Optic Communications", Feb. 1979

Figure 79

By the use of Snell's Law:

$$\sin \phi_i = \frac{N_2}{N_1} \sin \phi_r \quad (1)$$

An angle called the critical angle  $\phi_c$  is now defined:

$$\sin \phi_c = \frac{N_2}{N_1} \quad (2)$$

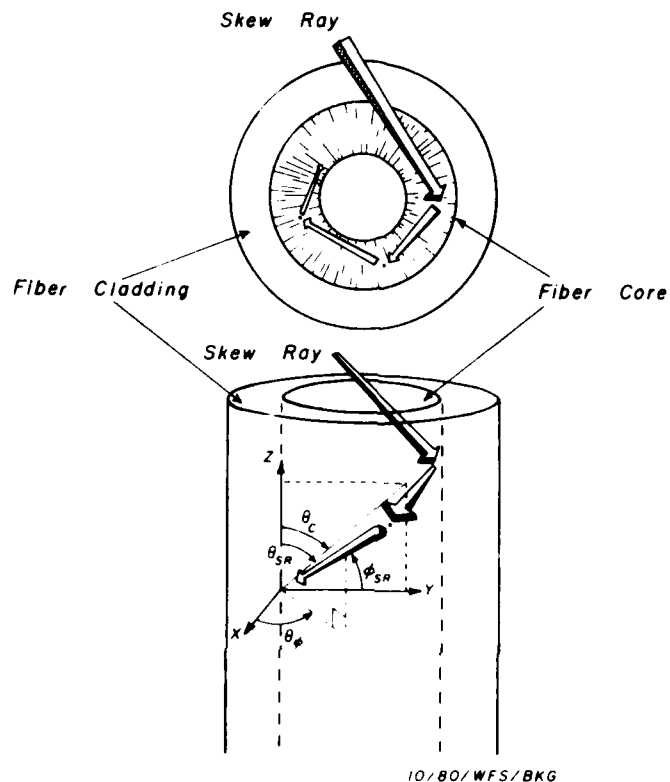
where  $N_2$  = index of refraction of the cladding

$N_1$  = index of refraction of the core

$\phi_i$  = angle of incidence of incoming light ray

If  $N_2$  is less than  $N_1$ , energy that is incident on the core-cladding boundary at an angle greater than  $\phi_c$ , will be totally

# SKEW RAY PROPAGATION OF LIGHT RAYS IN FIBER OPTIC



10/80/WFS/BKG

FIG. Bergstein, GWU (Wash. D.C.), "Fiber Optical Communications", Feb. 1979

Figure 80

reflected back into the core. Energy which has an angle of incidence less than the critical angle will be partially refracted into the cladding (Reference 7). These phenomena result in a flow of power in a direction parallel to the cladding-core interface. However, due to fiber imperfections, a small amount of light is reflected into the cladding, and

consequently a propagating field is creating in the cladding itself called the "evanescent" wave. Although its amplitude decreases as a function of the distance from the cladding-core boundary, this wave can couple into the cladding of an adjacent fiber, creating crosstalk between fibers under some conditions if considerable care is not maintained.

From the foregoing discussion of the critical angle, one can infer that there will be some angle beyond which light cannot be coupled into the fiber optic from a light source such as a LED or laser. This angle is known as the acceptance angle or maximum acceptance angle ( $\theta_{ACC}$  in Figure 79) and may be derived from Snell's Law as follows (References 7,9):

$$\begin{aligned}\sin \theta_{ACC} &= N_1 \sin \theta_c \\ &= N_1 \left[ 1 - \sin^2 \theta_c \right]^{\frac{1}{2}} \\ &= \left[ N_1^2 - N_2^2 \right]^{\frac{1}{2}}\end{aligned}\tag{3}$$

The above is called the "Numerical Aperture" (NA) of the fiber.

$$\begin{aligned}\text{Thus, Numerical Aperture (N.A.)} &= \sin \theta_{ACC} \\ &= \left( N_1^2 - N_2^2 \right)^{\frac{1}{2}} \\ &= N_1 \sqrt{2}\end{aligned}\tag{4}$$



where  $\left[1 - \frac{N_2}{N_1}\right]$ , a value defined as the "relative index difference." The power coupled into a fiber if reflection losses are neglected (Reference 7) is given by:

$$P(\text{Fiber}) = 2\pi A_s \int_0^{\theta_{\text{Acc}}} B(\theta) \sin\theta d\theta \quad (5)$$

where  $A_s$  is the area of the source and  $B(\theta)$  is the three-dimensional (spatial) radiation pattern of the source. The coupling efficiency,  $N_c$ , is defined as the power coupled into the fiber, divided by the total radiated power, and is expressed as:

$$N_c = P(\text{Fiber})/P(\text{Source})$$

$$= \frac{\int_0^{\theta_{\text{Acc}}} B(\theta) \sin\theta d\theta}{\int_0^{\pi/2} B(\theta) \sin\theta d\theta} \quad (6)$$

However, the radiation patterns of most LED's are similar to a Lambertian source (a source which appears equally bright from all viewing angles) so that  $\eta_o$ , the efficiency of light coupling into the fiber, can be written as:

$$\eta_o = (NA)^2 \quad (7)$$

This coupling efficiency can be greatly improved by the use of a coupling lens as may be deduced from the following set of equations and calculations.

From Figure 81 let:

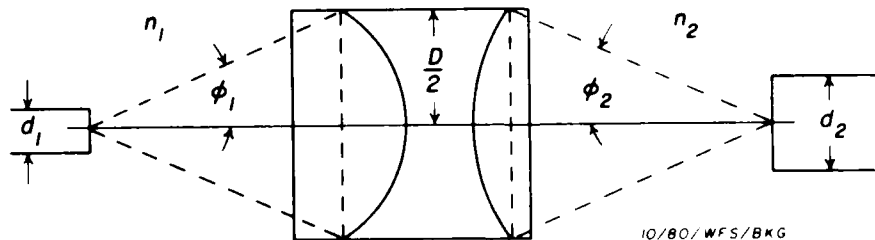
$d_1$  = diameter of source

$NA_1$  = numerical aperture of the lens (as seen from the source)

$d_2$  = diameter of the fiber bundle

$NA_2$  = numerical aperture of the fiber bundle

DIAGRAM OF COUPLING OF  
ELECTROMAGNETIC RADIATION INTO FIBER OPTIC FROM  
SOLID STATE LIGHT SOURCE via LENS



From L. Bergstein, GWU (Wash. D.C.), "Fiber Optic Communications", Feb. 1979

Figure 81

If,  $NA_1 = NA_2$  in Figure 81, then

$$d_1 \sin \theta_1 = d_2 \sin \theta_2 \quad (8)$$

$$\text{or } d_1(NA)_1 = d_2(NA)_2 \quad (9)$$

For a Lambertian source the coupling efficiency without a lens present is

$$\eta_c = (NA)_2^2 \quad (10)$$

With a lens present the coupling efficiency is

$$N_c(\text{lens}) = (NA)_1^2 \quad (11)$$

From Figure 81 we can derive:

$$\begin{aligned} (NA)_1 &= \sin \theta_1 = \sin\left(\tan^{-1}\left(\frac{D}{2F}\right)\right) \\ &= \frac{D/2F}{\sqrt{1+(D/2F)^2}} \end{aligned} \quad (12)$$

where D = diameter of lens

F = lens focal length

Let D = F (f/1.0 lens)

then if  $\theta_1 = 26.6^\circ$

$$(NA)_1 = \sin \theta_1 = \sin 26.6^\circ = 0.447$$

$$\therefore \underline{\eta_c(\text{lens})} = (\text{NA})_1^2 \approx \underline{20\%} \quad (13)$$

A practical fiber will have a numerical aperture of 0.2; thus, the coupling efficiency with no lens present will be

$$\underline{\eta_c(\text{no lens})} = (\text{NA})_2^2 = (0.2)^2 \approx \underline{4\%} \quad (14)$$

Thus it is apparent that a lens greatly improves the coupling efficiency of the light source into the fiber (Reference 7).

#### Propagation of Light in an Optical Waveguide

The velocity of light in a vacuum is  $3 \times 10^8$  meters/sec; however, as light travels through other materials such as water, gases and glass, its velocity appears to be considerably reduced. The ratio of the speed of light in a vacuum to the speed of light in a material such as glass is referred to as the "index of refraction" of the material, i.e.,

$$\text{Index of Refraction } N = \frac{\text{Speed of light in a vacuum}}{\text{Speed of light in a material}}$$

Although the above definition of the index of refraction of a material is widely used, it does not explain the reasons for the reduction in the velocity of light observed in media such as glass.

Recall that the displacement ( $y$ ) of a simple mass on a spring with one degree of freedom can be described by the equation:

$$\frac{W}{g} \frac{d^2 y}{dt^2} + C \frac{dy}{dt} + Ky = F_0 \cos wt \quad (15)$$

where  $\frac{W}{g} = \text{Mass}$

$-C \frac{dy}{dt} = \text{frictional force}$

$k = \text{spring modulus}$

$F_0 \cos wt = \text{disturbing force, usually periodic.}$

The solution of this second order differential equation describes the characteristics of the mass/spring system, including its resonant frequency, degree of damping and phase angle (Reference 12).

In a manner similar to that of Equation 15, the theory of wave mechanics states that the interaction of light photons and electrons may be described by a roughly similar heuristic model; that is, the electrons bound by interatomic forces can be conceptualized as a group of small masses under the influence of a restoring force similar to a spring. Consequently, the electrons interact with impinging light photons as if they were oscillators

with a characteristic resonant frequency ( $\omega_0$ ). Reference 13 presents an extremely lucid derivation of the index of refraction of a plate of glass using this "mass on a spring" concept, and solves Equation 15 to arrive at the following expression for the index of refraction of materials other than a vacuum:

$$n = 1 + \frac{Nq_e^2}{2\epsilon_0 m (\omega_0^2 - \omega^2)} \quad (16)$$

where:  $N$  = number of charge units per unit volume in a plate of glass.

$q_e$  = the charge of one electron

$m$  = the mass of an electron

$\epsilon_0$  = the permittivity of a vacuum ( $K_E \epsilon_0 = \epsilon$  the dielectric constant of a material)

$\omega_0$  = resonant angular frequency of an electron bound in an atom

$\omega$  = angular frequency of the radiation ( $\omega = 2\pi f$ )

Thus we see that the index of refraction depends on the number of electrons per unit volume of the material. Consequently a material containing substantial weight percentages of elements with high atomic number will exhibit a higher refractive index.

During their fabrication, optical quality glass fibers are grown in a manner similar to the techniques of epitaxial growth

employed in the manufacture of integrated circuits. The index of refraction of pure  $\text{SiO}_2$  is approximately 1.458; however, the refractive index of a glass fiber can be modified to either higher or lower values by diffusing into the fiber elements with higher or lower atomic number than the silicon, such as phosphorus or boron. This fabrication technique yields optical waveguides exhibiting highly controlled and accurate indices of refraction (References 7,9,10,11).

#### Material Dispersion

Upon entering a glass fiber, a light photon interacts with a bound electron in one of the atoms of the lattice structure of the fiber, causing the electron to oscillate in the same manner as a mass on a spring. The electron, which is a charged particle, emits radiation at the same frequency but at a slightly attenuated level, and delayed in time (phase shifted) by an amount equal to the duration required for the photon-electron interaction. As the frequency of radiation ( $\omega$ ) approaches the resonant frequency of the atomically bound electron, the denominator of Equation 16 approaches zero and the refractive index becomes very large. Thus, it is apparent that the refractive index of a given material assumes various values for different light wave frequencies. Consequently some light frequencies interact with larger numbers of electrons per unit propagation length than others, and are therefore delayed to a greater

extent per unit length of fiber optic material traversed.

Stated alternately, those frequencies with greater numbers of interactions per unit fiber length actually traverse the length of the fiber more slowly.\* This phenomenon is known as "material dispersion" and is in part responsible for "pulse spreading," a form of degradation of the frequency response of a fiber optic system. In glass this dispersion is positive; that is, low frequencies travel faster than high frequencies for wavelengths of light less than 1.27  $\mu\text{m}$ . The above described delay is called the "phase velocity," which will now be briefly discussed.

A monochromatic light wave  $f(t)$  propagating in the +Z direction can be expressed as (Reference 7):

$$f(t_1) = \text{Re} \{ A e^{i(\beta z_1 - \omega t_1)} \} = A \cos(\beta z_1 - \omega t_1) \quad (17)$$

where  $\omega$  = angular frequency of the electromagnetic wave ( $\omega = 2\pi f$ )

A = either a constant, or a function of the x and y coordinates

$\beta$  = the propagation constant =  $\frac{2\pi n}{\lambda}$

$\lambda$  = light wavelength

n = index of refraction

z = distance along the fiber axis in the direction of electromagnetic propagation

---

\*This is the phenomenon responsible for the rainbow.



This wave interacts with an electron, which oscillates, creating a new photon  $f(t_2)$ .

$$f(t_2) = A \cos (\beta z_2 - \omega t_2) \quad (18)$$

The "new" photon has the same frequency and shape as those of the incident photon, but it is shifted a distance  $z_2 - z_1$ , resulting in a "phase velocity"  $v_p$ :

$$v_p = \frac{z_2 - z_1}{t_2 - t_1} = \frac{\omega}{\beta}. \quad (19)$$

No electromagnetic wave is strictly monochromatic, for to be so it must exist forever, as is clearly demonstrated by the Theory of Linear (e.g., Laplace and Fourier) Transforms. Moreover, no radiation source presently known emits light of a single frequency; hence, each "wave packet" consists of many monochromatic waves (Reference 7), i.e.,

$$f(t) = \text{Re}\{A_1 e^{i(\beta_1 z - \omega_1 t)} + A_2 e^{i(\beta_2 z - \omega_2 t)} + \dots + A_n e^{i(\beta_n z - \omega_n t)}\} \quad (20)$$

Since the material index of refraction is different for each of these monochromatic waves, each will have its own propagation constant and thus each will travel through the optical waveguide at a characteristic velocity different from those of all other frequencies. The velocity of an infinitesimally narrow spectral width of a wave packet is known as its group velocity  $v_g$  (References 7,9,11):

$$v_g = \frac{d\omega}{d\beta} \quad (21)$$

For a single mode optical fiber the dispersion (G) can be expressed (Reference 7) in terms of the phase velocity ( $v_p$ ) and the spectral bandwidth ( $\Delta\lambda$ ):

$$G = - \frac{\lambda^2}{v_p^2} \frac{d^2 v_p}{d\lambda^2} \frac{\Delta\lambda}{\lambda} \quad (22)$$

Optical sources, particularly those employed in optical waveguide communication systems, have rather broad bandwidths. For instance, a LED source emitting at  $\lambda_0 = 10,000\text{\AA}$  has a spectral width of about  $350\text{\AA}$ , equivalent to a center frequency of  $3 \times 10^{14}$  Hertz and a bandwidth of  $9 \times 10^{12}$  Hz. A solid-state injection laser emitting light at  $10,000\text{\AA}$  has a spectral width of about  $10\text{\AA} = 3 \times 10^{11}$  Hz (Reference 7). Consequently, the material dispersion for a LED ( $\Delta\lambda = 350\text{\AA}$ ) and a solid-state injection laser ( $\Delta\lambda = 10\text{\AA}$ ) at a center wavelength of 0.9 micron are 10 nsec/km and 3.5 nsec/km, respectively. However, these changing effects as a function of frequency lead to some unexpected results. At  $1.27 \mu\text{m}$  the material dispersion becomes identically zero, and for longer wavelengths its sign is actually negative. At  $1.32 \mu\text{m}$  the value of the material dispersion in fact appears to cancel the waveguide dispersion described earlier, resulting in enormous feasible information transmission bandwidths (References 7,11). Recently this theoretical finding has been verified experimentally, when a

10.4 km long single mode fiber was used with lasers having wavelengths of 0.85  $\mu\text{m}$  and 1.293  $\mu\text{m}$ . At 1.293  $\mu\text{m}$  a pulse dispersion value of 3.9 psec/km/ $\mu\text{m}$  was observed (very close to the calculated value), while the measured pulse dispersion at a wavelength of 0.84  $\mu\text{m}$  was 100 psec/km/ $\mu\text{m}$  (Reference 8), or twenty-five times worse.

In 1973 the possibility of using the nonlinearity of the index of refraction in low loss fiber optics to compensate for pulse spreading was pointed out by Hasegawa and Tappert (Reference 15). This year (1980) this phenomenon has been studied and reported for the first time by Mollenauer, Stalen and Gordon, who reported observations and studies of pulse narrowing of 7 psec duration pulses to a minimum of 2 psec in a 700 meter length single-mode silica-glass fiber at a wavelength of 1.55  $\mu\text{m}$  (Reference 16). This wavelength of light was used in order to realize negative dispersion (reported by Mollenauer, et al., at -16 psec/ $\mu\text{m}$ /km), which is one of the requirements to realize pulse narrowing in an optical waveguide (negative dispersion implies that higher frequencies of light travel faster than lower frequencies). Another requirement for pulse narrowing in these media is that such studies must be carried out in a single mode low loss fiber.

It is known that the velocity of light of a given wavelength in a medium with a nonlinear refractive index is

a dependent function of the optical power (from the laser) above a certain threshold. To satisfy this third requirement for pulse narrowing, these investigators used a laser of sufficient power to exceed the power threshold. They reported that while the expected pulse spreading was observed at a laser output of less than 0.3 W, the pulse steadily narrowed at increased power levels until at a laser output power of 5 W, the 7 picosecond input pulse was narrowed to 2 psec. At power levels greater than 5 W the light pulse split into two or three pulses, a behavior which is characteristic of unique propagation waves called solitons, which represent solutions to the nonlinear Schrödinger equation well known in physics.

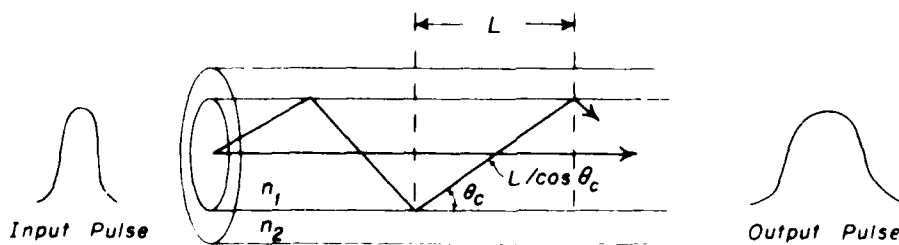
#### Intermodal Dispersion

From Figure 82 it can be understood that the meridional rays of the light beam travel through an optical waveguide by repeated reflections from the core-cladding interface at different angles with respect to the longitudinal axis. In fact, the ray moves from the core, and actually enters the cladding, where it encounters a lower refractive index; the velocity of the ray then increases, and it turns back in the direction of and re-enters the core. Clearly, the rays which subtend very small angles with respect to the waveguide longitudinal axis travel a much shorter path distance to the end of the waveguide than those rays which subtend angles approximately that of the

critical angle, since in effect these latter rays must "bounce back and forth" between "opposite" core-cladding interfaces many more times before reaching the far end of the fiber. Since two rays entering the fiber at different angles travel different distances at approximately the same velocity, the resulting differences in propagation delays through the fiber waveguide path result in a spreading of the input light impulse by the time it reaches the output. This phenomenon is called "pulse spreading due to intermodal dispersion," and, in conjunction with material dispersion, and waveguide characteristics, determines the impulse response and frequency response of the optical waveguide, and thereby its information carrying capacity in bits/second. It can be demonstrated (References 7,9,10,11) that for a step index optical waveguide the intermodal dispersion can be written as:

$$G_g = \frac{N_1}{C} \quad (23)$$

#### INTERMODAL DISPERSION IN STEP-INDEX FIBER OPTIC



From L. Bergstein, GWU/Wash D.C., "Fiber Optic Communications" Feb. 1974

Figure 82

where  $C$  = speed of light in a vacuum =  $3 \times 10^5$  km/sec

$N_1$  = index of refraction of the core

$$\Delta = \left[ 1 - \frac{N_2}{N_1} \right]$$

$N_2$  = index of refraction of the cladding

Thus the intermodal dispersion ( $G_g$ ) for a step index fiber can be calculated. A fiber with  $\Delta = .0018$  and  $NA = 0.09$  will exhibit an intermodal dispersion of 9 nsec/km, while an intermodal dispersion of 25 nsec/km will be manifested by a fiber having  $\Delta = .0050$  and  $NA = 0.15$ .

The intermodal dispersion for a graded index fiber can also be calculated (Reference 7) by the following expression:

$$G_g = \frac{n\Delta^2}{C} \quad (24)$$

where  $n = n(0)$  = the index of refraction of the fiber at its longitudinal axis. For  $n = 1.5$  and  $\Delta \leq 0.01$  or  $NA \leq 0.21$ ,  $G_g \leq 0.5$  nsec/km. Note that graded index fibers exhibit considerably lower pulse dispersion than step index fibers.

### Modes

If Maxwell's equations are solved for a cylindrical waveguide, a set of J-type Bessel functions of order  $\mu$  are realized, such that in the core of a step index fiber,  $E_z$ , the electric

field propagating along the longitudinal axis of the fiber (the "Z" direction) and  $H_z$ , the magnetic field, may be expressed as

$$\begin{bmatrix} E_z \\ H_z \end{bmatrix} = \begin{pmatrix} A \\ B \end{pmatrix} J_v(UP) e^{i v \phi} \quad (25)$$

where  $U^2 = (K_1^2 + \beta^2)$

$K_1 = \frac{2\pi n}{\lambda}$  the propagation constant

$\beta = z$  component of propagation vector

A and B = Arbitrary constants

After considerable mathematical manipulation it can be demonstrated that there are only certain discrete propagation modes which can exist. These modes, which can be categorized as the Transverse Electric (TE( $E_z=0$ )) and Transverse Magnetic (TM( $H_z=0$ )) modes, are radially symmetric. There are also hybrid modes, which are designated  $HE_{vm}$  or  $EH_{vm}$ , depending upon which of the two fields, magnetic or electric, makes the larger contribution to the transverse field. Each mode is also characterized by specific polarization of its electric field (Reference 11). One of the hybrid modes, designated  $HE_{11}$ , is of special interest because it forms the theoretical basis for a single mode waveguide. By adjusting the parameters of the optical waveguide, it is possible to suppress all propagation modes except  $HE_{11}$ . Each waveguide exhibits a "V" parameter which uniquely characterizes its propagation characteristics at a particular wavelength. The value of the V parameter is given by:

$$V = \frac{2\pi a}{\lambda} \sqrt{n_1^2 - n_2^2} \quad (26)$$

$a$  = constant

$n_1$  = index of refraction of the core

$n_2$  = index of refraction of the cladding

A  $V$  value of 2.405 or less insures that all modes except  $HE_{11}$  will be suppressed while preserving single mode propagation as the only transmission mode, and thereby facilitating a large information carrying capacity (reference 11). However, since  $V$  is a function of  $a$ , the single mode waveguide must be designed for a given optical frequency (References 7,9,10,11). As  $V$  increases, the maximum number of modes which can propagate also increases up to several thousand in some multimode waveguides. Equations 27 and 28 demonstrate that the total number of propagating modes in a step index fiber is half that of a graded fiber; hence, the graded index fiber (i.e., with  $\alpha = 2$  in Equation 27) will accept only half the light of a step index fiber.

The number of propagating modes ( $N$ ) for a graded index fiber (References 7,11) is given by:

$$N = \left(\frac{\alpha}{\alpha+2}\right) k_0^2 a^2 n^2(o) \cdot = \frac{1}{4} V^2 \quad (27)$$

where:  $\alpha$  = index profile shape parameter

$$k_0 = \frac{2\pi}{\lambda} n$$



$n(o)$  = refractive index of core

$a$  = core radius

$V$  = waveguide "V" parameter (from Equation 26)

$$V = n^2(o) - n^2(a) / 2n^2(o)$$

For a step index fiber the number of propagating modes is simply

$$N = \frac{V^2}{2} \quad (28)$$

#### Losses Caused by Absorption and Other Phenomena

Recently, very low loss fibers have been fabricated exhibiting attenuations of 0.47 dB/km at  $\lambda = 1.2 \mu\text{m}$  and 0.2 dB/km at  $\lambda = 1.55 \mu\text{m}$ . The causes of absorption losses in fiber optics are 1) intrinsic absorption by the material; 2) impurity absorption; and 3) atomic defect absorption. The most serious cause of attenuation of light in fiber optics is absorption by impurities such as OH ions (which is especially severe at 725, 825, 875, and 980  $\mu\text{m}$ ) and to a lesser extent by metal ion impurities such as Fe, Cu, V, and Cr (Reference 11). Atomic defect absorption can be caused by exposure of the glass to radiation; however, the type of glass used in the fiber largely determines the degree of radiation damage incurred. As an example, loss factors of 20,000 dB/km have been observed in conventional fiber optic glasses exposed to relatively low level gamma radiation

of 3,000 rads, whereas the attenuation in a germanium doped glass has been measured at only 16 dB/km for a radiation exposure level of 4,300 rads.

All transparent materials exhibit local spatial variations in the density of atoms and hence of the refractive index within the material. It is believed that this phenomenon, which is called Rayleigh scattering, represents the fundamental limit of minimum attenuation in an optical waveguide. Scatter due to inhomogeneities of the same approximate size as the wavelength of the propagating light is called Mie scattering, while that due to small nonlinear effects due to the interaction between the optical field and the fiber is called Stimulated Ramon and Brillouin scattering (References 7,11). Scattering can also be caused by small geometrical variations in the core diameter of the fiber, which cause energy to shift among guided modes. The losses due to microbending of the waveguide and other forms of mechanical distortion result in "mode coupling," an advantageous phenomenon which actually decreases modal pulse spreading and thus enhances the impulse response of the waveguide (Reference 7).

Losses due to bending of the fiber are also important (Reference 7); the minimum allowable radius of curvature,  $R_{\min}$ , of a bend in a step index fiber optic is given by:

$$R_{\min} = \frac{2R^2}{(NA)^2} \quad (29)$$

where: NA = the numerical aperture

n = index of refraction of core

r = radius of fiber

For example, if NA = 0.2, n = 1.5, and r = 50  $\mu$ m,  $R_{\min}$  would be approximately 5.5 mm.

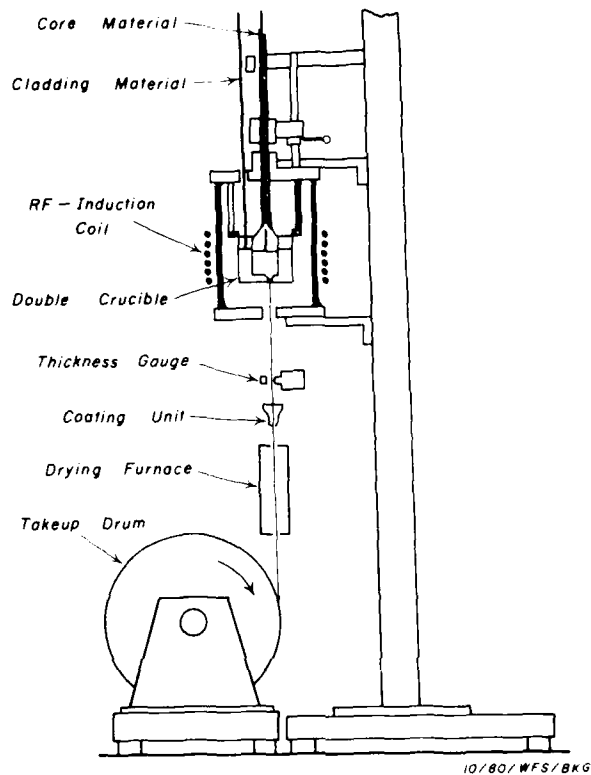
Recently an additional source of high frequency noise has been observed (reference 11) called modal or speckle noise, which appears to be determined in part by the design of the splices, connectors and source/detector connectors of an optical waveguide system. This form of noise is thought to be generated when the light from a coherent laser source splits into different modes in a multimode fiber.

#### Fabrication of Optical Fibers

Several different methods have been used to manufacture optical waveguides, including a chemical vapor deposition technique, a stratified melt process, and the processes depicted in Figure 83, which are known collectively as the double crucible method. As shown in Figure 83, the double crucible continuously provides fresh quantities of raw material glass for the core and cladding to a pair of coaxially aligned crucibles which are

induction heated to a high temperature. The fiber is pulled from the bottom of this structure, then through a thickness gauge and a drying furnace, and is then coiled on a spooling drum. Fibers of several kilometers in length have been manufactured in this way. The British use the stratified melt process, in which glasses of two indices of refraction are placed together and melted. The glass with the lower refractive index possesses a lower specific gravity and floats to the top of the melt. The higher refractive index glass is then actually pulled through the upper layer of low index glass, which adheres to the inner core to form the cladding. Very low loss fibers (2-4 dB/km) are realized in this way, because the details of the stratified melt process facilitate very low contamination at the core-cladding interface (Reference 7). In addition, this process can be adopted to a superior clean room environment in comparison to the other techniques. Lastly, the chemical vapor deposition process realizes glass fibers with attenuation factors on the order of 0.47 to 1 dB/km at 1.2  $\mu$ m and 0.95  $\mu$ m, respectively (Reference 7). On the other hand, the technology for the double crucible method has been available for many years and the dimensions of the fibers can now be controlled to an accuracy of 0.3%, thus minimizing splicing and coupling losses.

SCHEMATIC OF MECHANISM FOR  
FABRICATION OF OPTICAL FIBERS USING  
DOUBLE CRUCIBLE METHOD



From: L. Bergstein, GWU (Wash. D.C.), "Fiber Optical Communications", Feb. 1979

Figure 83

### Splicing of Optical Fibers

The two most thoroughly developed methods of fiber splicing employ either mechanical techniques or thermal fusion of fiber ends. Fusion splices result in lower losses but have proven (thus far) difficult to realize under field conditions;

consequently a large number of mechanical splices have been installed by field crews (References 7,9).

The method of splicing is as follows: 1) fiber ends are in some way prepared (cleaned, heated, and/or polished); 2) the two fibers are brought into a precise coaxial contact position; and 3) the positions are fixed. For a mechanical splice, grooves, tubes or pins are used to facilitate alignment; the position is then stabilized with epoxy (References 7,9,10,11). The Atlanta Georgia Bell test facility has successfully spliced a linear array of fibers by controlled fracturing of the fiber ends followed by fiber end alignment via a grooved substrate (References 7,10).

Two predominant classes of fiber splicing losses have been identified. "Intrinsic losses" are due to core area mismatch, numerical aperture mismatch or profile mismatch of the two waveguides to be spliced. "Extrinsic loss" is caused by end separation (i.e., the fiber ends are not butted against one another), angular misalignment, or lateral offset (radial displacement). Radial displacement and end separation of the fibers to be spliced can easily result in 4 dB losses. Physical distortion of the fibers, Fresnel reflections (due to poor end finishing), stresses on fiber joints or dirt can also be responsible for excessive losses at fiber splices (References 7,11).

The insertion losses ( $L_c$ ) due to intrinsic losses, to the mismatch of the fiber core, to mismatches of the numerical aperture NA or the index profiles of the fibers can be expressed as:

$$L_c = -10 \log \left( \frac{r_S(r_R+2)}{r_R(r_S+2)} \right) - 10 \log \left( \frac{a_R}{a_S} \right)^2 - 10 \log \left( \frac{NA_R}{NA_S} \right) \quad (30)$$

where:  $a$  = radius of core

$r$  = index shape parameter of fiber

NA = numerical aperture of fiber

The subscripts S and R refer to the "transmitting" and receiving fibers, respectively.

Engineers responsible for fiber optic cable installation crews have communicated to the author of Part III of this report (W.F.S.) that they often splice in the field by simply breaking off the ends of the fibers to be spliced, and heating them in a flame until a simple lens appears on the end of each fiber. The newly treated fiber ends are then butted against one another and stabilized in position by one of the mechanical means discussed earlier. The newly and simply created lens systems facilitate a minimal loss of light due to the splicing procedure.

Single mode fibers are especially difficult to splice in a manner which retains low insertion loss. However, it is possible to splice a single mode fiber with losses of 0.5 dB by using preferentially etched grooves in a silicon substrate to insure axial misalignment of no more than 1  $\mu$ m. Thermal fusion of the fiber ends is then employed, resulting in fiber splices exhibiting coupling losses of <0.25 dB. Recently a "prefusion" method has been developed which results in splices exhibiting 0.09 dB losses, and requires only a few seconds to complete (Reference 10).

#### Electroluminescent Sources for Optical Communication Systems

When a electroluminescent solid-state diode (PN junction) is forward biased, electrons and holes are injected into the P and N type regions, respectively. The current/voltage relationships are described by the following well-known equation:

$$I = I_s \left[ \left( \exp \frac{qV}{aKT} \right) - 1 \right] \quad (31)$$

where:  $I_s$  = saturation current  
 $K$  = Boltzman's constant  
 $T$  = Absolute temperature  
 $V$  = Bias voltage  
 $q$  = Electron charge  
 $a$  = a constant, between 1 and 2



The electrons and holes can recombine radiatively (i.e., the emitted photon energy  $h\nu$  is approximately equal to the material bandgap energy  $E_g$ ). Electrons and holes also can recombine in a nonradiative manner, in which case the emitted energy is in the form of heat (References 7,11). Radiation energy from these devices is either spontaneous or stimulated. Diodes which emit radiation by spontaneous emission are called "Light Emitting Diodes" or simply L.E.D.s, while those emitting light by stimulated emission are called "Lasers."

Each of these devices exhibits a unique set of physical characteristics, which may be either advantageous or disadvantageous depending on the desires of the user. Light is emitted from a Laser Diode only when a certain threshold current is exceeded, whereas a L.E.D. possesses no such minimum threshold current. The L.E.D. is easier and less expensive to fabricate and exhibits a lower temperature dependence than does the laser. The width of the emission spectrum of a L.E.D. is on the order of 300 to 500 Angstroms, compared to 1 to 10 Angstroms for a solid-state laser (lasers have been fabricated at Bell Laboratories which exhibit only a  $0.1 \text{ \AA}$  spectral width). Although the spectral width of the source is not critical for systems involving only a few meters of fiber optic cable, for optical communication systems requiring high data rates over several kilometer distances the use of a L.E.D. source can result in serious material dispersion, thus causing

a degradation of the system frequency response even though the frequency characteristics of the L.E.D. itself may be adequate. In addition, the radiance of a L.E.D. is less than that of a solid-state laser, and thus smaller quantities of power are coupled into the fiber. The modulating frequency capability of a L.E.D. is limited by carrier lifetime to approximately 200 MHz, even when specially doped material is employed in the manufacture of the device. Conversely, the laser can be modulated at rates above 1 GHz if D.C. biased at the threshold current, since electron-hole recombination is accomplished when a photon forces an electron from the conduction band into the valance band (referred to as stimulated electron-hole recombination). The L.E.D. emission energy is approximately equal to the material bandgap ( $E_g = hc/\lambda$ ), while that of a laser is  $h\nu < E_{fc} - E_{fv}$ , where  $E_{fc}$  = quasi-Fermi level in the conduction band and  $E_{fv}$  = quasi-Fermi level in the valance band (Figure 84). The Fermi level is the highest level of energy at which there is a finite probability that the energy level will actually be occupied by an electron (Reference 17). The L.E.D. is much less temperature sensitive than the laser; the laser threshold current may double between 20° and 70°C, whereas the spontaneous emission of a Double Heterostructure L.E.D. decreases by only a factor of two from room temperature to 100°C. Since the laser thus requires special temperature compensation circuits or optical feedback to assure its operational integrity, the L.E.D. is preferred over the laser if all other considerations are equal (References 7,9,10,11).

## Light Emitting Diodes

Presently available light emitting diodes and lasers suitable for optical communication systems emit light in the region of 715-905 nm, i.e., between 1 and 1.55  $\mu\text{m}$ . The latter wavelength band takes advantage of the very low loss, as well as low or even negative material dispersion "windows" in the transmission spectrum of glass in the regions of 1.3 and 1.5  $\mu\text{m}$ . Those devices which emit light between 715 and 905 nm are fabricated from  $\text{Al}_x\text{Ga}_{(1-x)}\text{As}$  on a GaAs substrate. The mole fraction of Al in the compound controls the peak wavelength at which these devices emit light. The emission wavelengths between 1 and 1.5  $\mu\text{m}$  are realized by devices made with  $\text{In}_x\text{Ga}_{(1-x)}\text{As}$  on a GaAs substrate;  $\text{In}_x\text{As}_{(1-x)}\text{P}$  on an InP substrate; or  $\text{GaAs}_x\text{Sb}_{(1-x)}$  on a GaAs substrate (Reference 11).

The various configurations of L.E.D.s, their packages, and physical characteristics are depicted in Figure 85. The two diode configurations usually incorporated in an optical communications system are surface emitters and edge emitters. The surface emitters have their active (light emitting) region close to a heat sink (to accommodate higher current and thus increased light output). A well is etched through the GaAs substrate to facilitate installation of the polished end of a fiber, sometimes with etched lenses. The edge emitter structures use partial waveguiding to

facilitate increased light output. The surface emitters exhibit a Lambertian pattern, while the edge emitters have a narrow active region which reduces beam divergence. Figure 85 also compares the different L.E.D. configurations and structures in regard to the size of active areas, total and coupled radiated power, quantum efficiency and transmission bandwidths (Reference 7).

# ENERGY BAND DIAGRAM OF POPULATION INVERSION IN INJECTION LASER DIODE

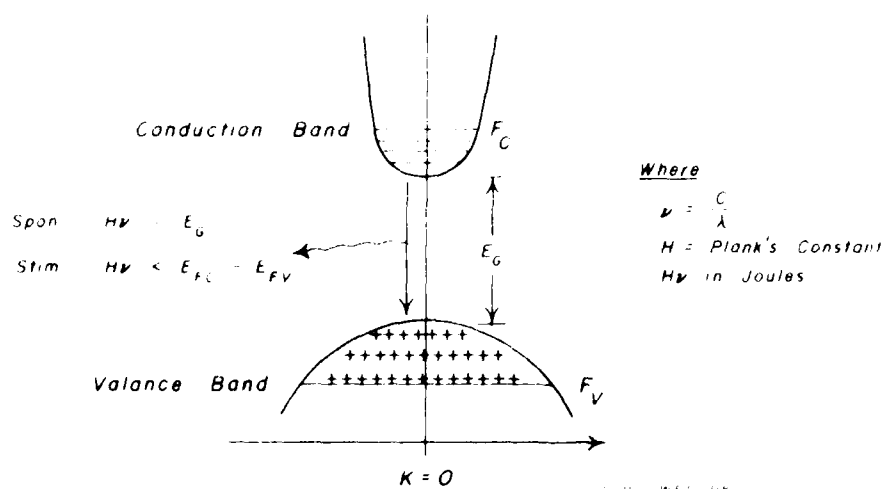
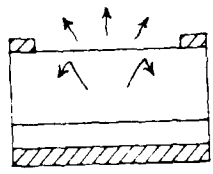
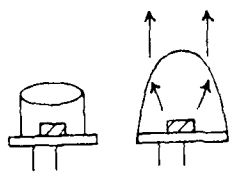
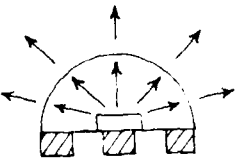
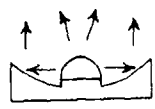
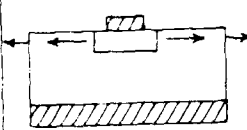
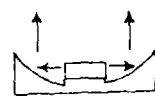
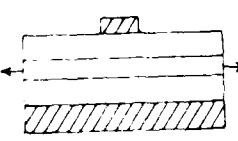
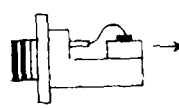
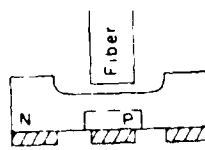
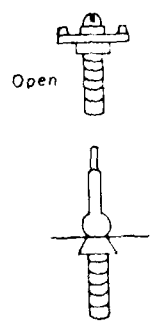
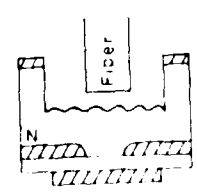


Figure 84

TYPE	STRUCTURES	PACKAGE	AREA (MM <sup>2</sup> )	TOTAL RADIATED POWER (MW)	COUPLED POWER (MW) SINGLE BUNDLE	EXTERNAL QUANTUM EFF	BANDWIDTH (MHZ)
Planar			8-15	1 to 3	1 3000	.2%	30 to 50
Dome			6-12	2 to 50	5 1000	5%	30
Edge			2-4	1 to 5	10 1000	2%	30
OH Edge			.003	.3 to 1.0	20 --		150
Burros			.002 to .03	0.5 to 10	60 --	.4%	60
			.002 to .03	0.5 to .10	200 --	2-7	45

From L. Bergstein, GWU (Wash. D.C.), "Fiber Optical Communications", Feb. 1979

Figure 85

COMPARISON OF L.E.D. TRANSMITTERS FOR FIBER OPTICS

The frequency response of the L.E.D. structure is governed by its capacitance and its mean carrier lifetime. The latter can be calculated as follows:

$$\tau = \frac{\tau_r \tau_{nr}}{\tau_r + \tau_{nr}} \quad (32)$$

where  $\tau_r$  and  $\tau_{nr}$  are the carrier lifetimes of those carriers which take part in radiative and nonradiative recombination, respectively. The frequency response of the L.E.D. can be improved to a maximum of approximately 200 MHz by varying the dopant concentration. Doping of GaAs with Si at a concentration of approximately  $10^{17}$  atom/cm<sup>3</sup> results in  $\tau_r = 27$  nsec, while doping of GaAs with a concentration of  $10^{19}$  atom/cm<sup>3</sup> of Ge results in  $\tau_r = 1-2$  nsec (References 7,11).

### Injection Laser Diodes

The practical realization of solid-state laser diodes capable of operation at or above room temperature was achieved through the successful fabrication of the AlGaAs/GaAs heterojunction in 1969. As depicted in Figure 86, the heterojunction consists of four layers of  $\text{Al}_x\text{Ga}_{(1-x)}\text{As}$  grown epitaxially on a substrate. These four layers consist of a contact layer, a recombination region and two confining regions (a P type and an N type), thereby completing the PN junction. The confining regions are composed of material having a higher bandgap energy

# AlGaAs STRIPE-CONTACT LASER (ILD)

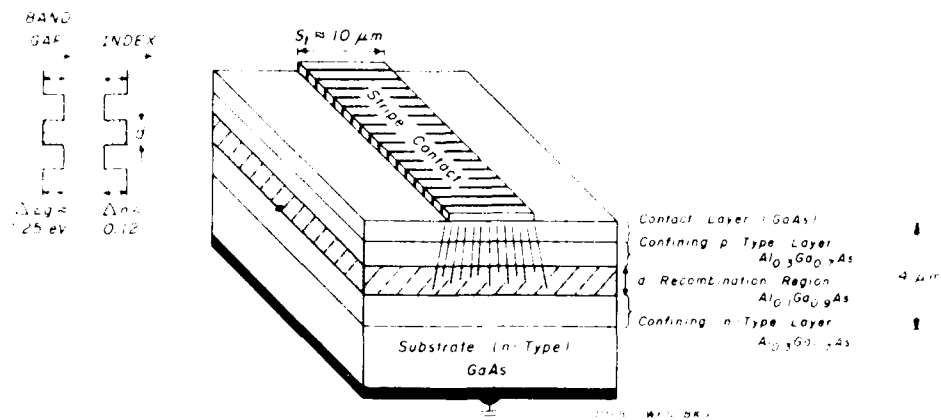


Figure 86

( $E_g$ ) than the recombination or active region, thereby serving as potential barriers at the active region interfaces (i.e., the injected carriers are thus confined in the active regions). The  $\text{Al}_x\text{Ga}_{(1-x)}\text{As}$  confining material also exhibits a lower refractive index than the material in the active region, thereby creating an optical waveguide as well. The active region is actually an electromagnetic resonating Fabry-Perot chamber, with mirror facets at both ends of the device formed by cleaving the crystal along its crystal planes (References 7,11,19). The approximate thicknesses of the heterojunction are 1) Active region:  $0.05\text{--}0.3 \mu\text{m}$ ; 2) Confining regions:  $1\text{--}3 \mu\text{m}$ ; 3) Contact layer:  $3\text{--}4 \mu\text{m}$ ; and 4) Substrate:  $50\text{--}100 \mu\text{m}$ .

When the laser diode is forward biased, electrons and holes flow from the P and N doped areas respectively, into the active area and are trapped there by the confining layers. Electron-hole recombination then occurs, creating spontaneous light emission. At a specific value of diode current called the threshold current (between twenty and several hundred milliamps, depending on the device design and the operating temperature) sufficient electrons are injected into the active region to fill completely the lower energy state of the conduction band up to the quasi Fermi level for electrons (Figure 84). An equal number of holes are also injected (thereby maintaining charge neutrality in the active region) and thus the valance band is empty of electrons up to the quasi Fermi level for holes. Photons in the active region (newly created by the electron-hole recombination) with an energy,  $E$ , (with  $E_g < E < (F_c - F_v)$ ) cannot be absorbed because the valance band states are empty and the conduction band states are full, thus creating a population inversion." Consequently, a photon can induce or "stimulate" electrons to "fall downward" to lower energy states from the conduction band to the empty valance band states, thereby producing photons with the same wavelength as the "stimulating" photon, which is itself not absorbed in the process. Therefore, the number of photons with the same wavelength increases, and light amplification by stimulated emission is realized. Since the density of the photons is greatest at the peak of spontaneous emission, this value of  $\lambda$  is the wavelength of peak laser output



power. Since, as described above, these devices achieve population inversion by the injection of electrons and holes into the recombination region, they are called "Injection Laser Diodes" or simply ILDs (References 7,11).

### Laser Modes

As the active region of the laser diode is an optical waveguide, it is characterized by electromagnetic modes, as discussed in the optical waveguide section of Part III of this report. These modes can be separated into two sets, one with transverse electric (TE) and one with transverse magnetic (TM) polarization. The modes of each set are referred to by mode numbers, which define the number of field variations  $m$ ,  $s$  and  $q$  in the longitudinal, lateral, and transverse axis, respectively. The longitudinal modes, which are allowed to propagate between the Fabry-Perot faces in the junction plane, are determined by the average index of refraction ( $\bar{n}$ ) as well as the material dispersion. The spacing of these modes is on the order of several Angstroms ( $\text{\AA}$ ), and is given by:

$$\frac{1}{\Delta q} = \frac{-\frac{1}{2}L}{2L(\bar{n} - \frac{dn}{d\lambda})} \quad (33)$$

where  $q$  = longitudinal wave numbers

$L$  = length of resonating cavity

The transverse modes of an ILD are in the lateral and vertical directions, while the lateral modes are in the plane of the junction and are separated by approximately 0.1 to 0.2  $\text{\AA}^\circ$  (References 7,11).

In the vertical direction the light is guided by the lower refractive index layers on the "top" and "bottom" of the active layer, i.e., by the confining layers. By restricting the width of the active region of the laser to less than one micrometer, it is possible to achieve a waveguide condition which allows the excitation of only the fundamental mode; thus the far-field radiation pattern of the laser beam will consist of a single lobe in a direction perpendicular to the junction, a pattern which facilitates improved optical coupling between the laser and a fiber.

The following relationship allows a calculation of the electric field ( $\tau$ , which is transmitted through the mirror at the end of the Fabry-Perot interferometer chamber (Reference 7):

$$\tau = (T^2 e^{iKd}) + (T^2 r^2 e^{i3Kd}) + T^2 r^4 e^{i5Kd} + (T^2 r^6 e^{i7Kd}) + + + \dots \quad (34)$$

where  $T$  = transmission coefficient

$r$  = reflection coefficient

$e$  = base of natural log system - 2.71828 . . .

such that:

$$|T|^2 + |r|^2 = 1$$

$d$  = resonating cavity "separation"

$k = \frac{2\pi n}{\lambda}$  = propagation constant for wavelength  $\lambda$  and index of refraction  $n$ .

From the above relationship it is also possible to calculate the spectral width of the emitted laser beam. In general there is an inverse relationship between the magnitude of the cavity separation and the laser spectral width. The Helium Neon Laser, with a cavity separation of approximately 60 cm, exhibits a spectral width of only .003A°, while an injection laser with a cavity separation of 100  $\mu$ m exhibits a spectral width on the order of 10A° (Reference 7). It should be noted that other factors in addition to cavity size affect spectral width. For example, the allowed energy levels for electron-hole recombination in the solid-state device overlap one another, resulting in a greater spectral width of the emitted beam than exhibited by the gas laser, in which the energy levels tend to be relatively more discrete.

The lateral dimensions of the waveguide of an injection laser diode, if fabricated without the stripe contact shown in Figure 86, actually alter with changes in current. Thus, the waveguide becomes smaller or larger in this axial direction

during each "cycle" of signal modulation due to current spread in the diode, in turn causing lateral mode instability. The stripe geometry corrects this problem either wholly or in part, depending to some extent on the sophistication of the technique used to fabricate the stripe contact. The most effective way to eliminate completely the current spread problem is via a proton implantation approach. In this procedure, high energy protons convert all but the stripe contact in the contact layer of the laser to a very high resistivity material ( $10^6$  ohms-cm). An injection laser diode with a very stable transverse mode and high linearity may be fabricated in this manner (References 20,21).

When a current pulse with a very rapid risetime is applied to a laser diode, a delay time ( $t_d$ ) is observed before laser oscillations begin. This delay can be approximately calculated by:

$$t_d = \tau \ln \left( \frac{I}{I - I_{th}} \right) \quad (35)$$

where  $\tau$  is the carrier lifetime ( $\approx 2-5$  ns). This delay is the time required for the current flowing through the diode to "build" the injected current density to a level great enough for electron-hole population inversion to occur. However, this delay may be minimized (Reference 18) by superimposing the current pulse on a D.C bias current  $I_b$ , in which case  $t_d$  becomes

$$t_d = \tau \ln \left( \frac{I - I_b}{I - I_{th}} \right) \quad (36)$$

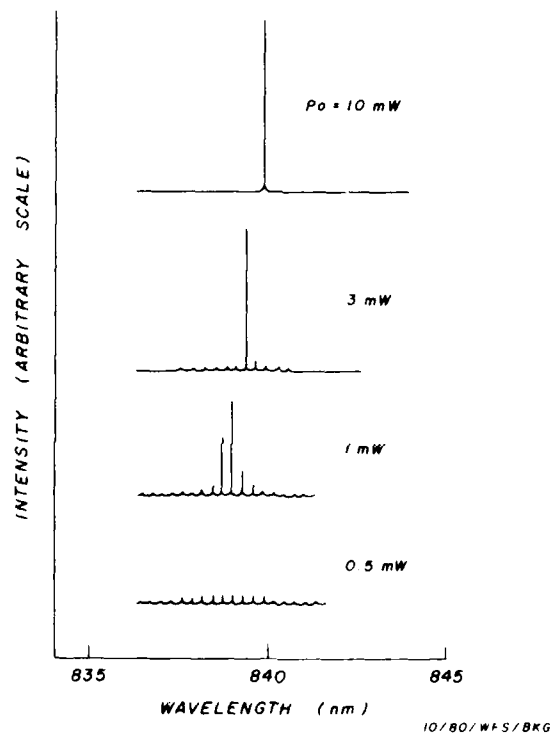
where  $I_{th}$  = threshold current.

During fast pulse operation the ILD tends to oscillate in several longitudinal modes for approximately 100 nsec at the onset of each pulse. To correct this phenomenon the device may be biased to a current level approximately 1.2 times the threshold current when high-speed operation is required. Also observed during fast pulse operation is a relaxation oscillation at a frequency of 1 GHz or greater superimposed on the laser light pulse output, a phenomenon which varies with the level of injection current and from device to device (Reference 18).

Figure 87 shows the emission spectra of a Hitachi HLP 1000 diode with the output power increased in steps from 0.5 to 10 mW. Note that at an output power of only 0.5 mW, many longitudinal modes are observed. As the laser power is increased to 2 or 3 mW, the output appears to concentrate into a single longitudinal mode at 840 nm. Nonetheless, closer study reveals that even at 10 mW output power other longitudinal modes exist, albeit at very small intensities, and spaced at roughly 0.3 nm wavelength intervals both above and below that of the primary longitudinal mode. Although not clearly depicted in Figure 87, the output light intensity from these devices increases as input power ( $P_o$ ) is increased. For instance, the

light output of this laser with  $P_O = 10$  mW is drawn at 1/10 the vertical scale of that used for  $P_O = 1$  mW.

TYPICAL EMISSION SPECTRA  
OF HITACHI HLP-1000 LASER DIODES AT  
VARIOUS OUTPUT POWER LEVELS



Revised From Hitachi Laser Diode Application Manual, p. 15

Figure 87

Because both the bandgap energy and the refractive index are temperature dependent, it follows that the emission spectrum

of the ILD is also temperature dependent. As the temperature of the ILD is raised, each longitudinal mode and the peak wavelengths shift to longer wavelengths at a rate of approximately 0.06 nm/K and 0.3 nm/K, respectively (Reference 18).

Finally, since the emitted wavelengths of ILDs are invisible and also maybe harmful to the human eye, various devices have been suggested by the manufacturers of these devices to allow visualization of the beams generated by injection laser diodes, including infrared sensitive ITB cameras of the silicon-vidicon type, infrared-to-visible image converters, and special IR-phosphor plates manufactured by Kodak (Reference 18).

In summary, several of the general physical characteristics of GaAlAs injection laser diodes are presented in the following table:

Structure	$\text{Ga}_{(1-x)}\text{Al}_x\text{As}$ Heterostructure
Chip Size	350 x 250 x 100 $\mu\text{m}$
Wavelength	800 to 890 nm
Spectral Width	0.2 to 5 nm
Source Size	0.5 to 30 $\mu\text{m}^2$
Beam Divergence:	
Parallel to Junction	5°-30°
Perpendicular to junction	30°-50°

#### Operating Optical

Power	1-10 mW
Power Coupled into	
Fiber	0.1-1 mW
Threshold Current	20-200 mA
Drive Current	5-50 mA
Forward Voltage	1.5-3 V
Rise/Fall Time	0.1 to 1 nsec
Lifetime	10,000 Hours (several recent designs stable to 100,000 hours)

#### Optical Detectors for Optical Waveguide Systems

Photodetection is the conversion of optical power into an electrical current. Several types of detectors are available for consideration, including photomultiplier tubes, photocathode tubes, photoconductors, PIN photodiodes, and avalanche photodiodes.

Several fundamental requirements can be defined (Reference 7) for photo detectors to be used in an optical communication system: 1) high response to incident optical energy; 2) adequate bandwidth to respond to an optical signal carried by the fiber optic; 3) minimum internal noise; 4) temperature insensitivity; and 5) ease and practicality of use with a fiber optic system (small size, compactness, and ease of coupling to fiber).

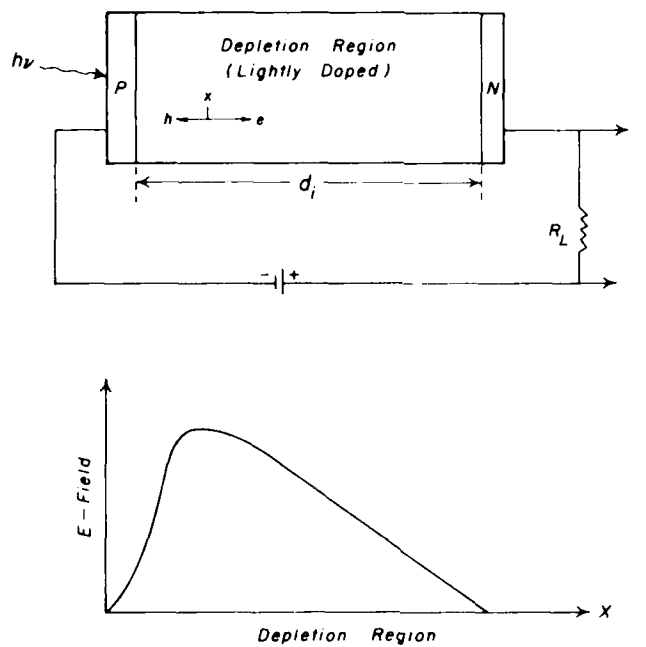


Consideration of these requirements has resulted in the selection of two types of silicon semiconductor device, both of which are basically reverse-biased PN diodes. One of these is referred to as a PIN photodiode, and the second as an avalanche photodiode (APD). Because of space limitations, only a few of the major physical characteristics of these photodiodes will be discussed in this report; a wealth of available information regarding amplifier characteristics and noise of the detection system will only be briefly mentioned.

#### PIN Photodiodes

The PIN photodiode is structured as shown in the upper panel of Figure 88, with a very thin P-type layer to allow high transmission of incident light through the P-layer to the depletion region. The depletion region, which contains an electric field as shown in the lower panel of Figure 88, is formed by immobile donor atoms on the N-side of the junction and immobile acceptor atoms on the P-side. This depletion region is such a very lightly doped N layer that it is usually considered to be intrinsic (that is, to be essentially pure silicon with no impurities). As depicted in the upper panel of Figure 88, a highly doped N layer is used to facilitate a good contact on the opposite side of the depletion region from the P layer. The device is back biased at a voltage level (usually in the range of 20 to 100 volts) as close to diode

# DIAGRAM AND ELECTRIC FIELD PLOT OF PIN PHOTODIODE



10/80/WFS/BKG

From *Fundamentals of Optical Fiber Communications*, ed. by M. K. Barnasik,  
Academic Press 1976, p. 159

Figure 88

breakdown as is practical (Reference 7). Because the photodiode exhibits only a junction capacitance,  $C_j$ , it can operate at higher modulation rates than the L.E.D. and laser diode sources described above, which are forward biased and hence exhibit "excess charge" capacitances in addition to their junction capacitances. The photodiode junction capacitance can be calculated by the following relationship:

$$C_j = \epsilon_0 \epsilon_r \frac{A}{d} \quad (37)$$

where  $\epsilon_0$  = permittivity of free space

$\epsilon_r$  = relative dielectric constant of diode material

A = area of junction

d = depth of junction

Thus,  $C_j$  can be reduced and the frequency response improved by increasing d. PIN devices display junction capacitances of 1-7 pF, and risetimes frequently on the order of one nsec or less (References 7,11).

Light enters the PIN diode, traverses the P layer, and is absorbed in the depletion or "intrinsic" region where it excites a bound electron into the conduction band and thus creates an electron-hole pair. These carriers then separate under the influence of the high electrostatic field gradient, resulting in a displacement current in the circuit. Although any light which passes through the depletion layer and is absorbed in the N layer will also create electron-hole pairs, these pairs will recombine very quickly due to the high N doping and short carrier lifetimes of the N layer and hence will not contribute to the photocurrent. The photo current  $I_{ph}$  can be expressed as follows:

$$I_{ph} = \frac{e \eta P_{opt}}{h \nu} \quad (38)$$

$\eta$  = detector quantum efficiency (fraction of incident photons which liberate electrons)

$e$  = electronic charge

$h$  = Planck's constant =  $6.63 \times 10^{-34}$  J-sec

$\nu$  = optical frequency =  $\frac{c}{\lambda}$

$\frac{P_{opt}}{h \nu}$  = average number of incident photons/unit time

$\frac{I_{ph}}{e}$  = average number of electron-hole pairs generated per unit time

$\frac{I_{ph}}{P_{opt}}$  = "responsitivity" of the device

"Responsitivity" is the average emitted current divided by the average incident optical power and is expressed in amps/watt. A PIN diode with 100% efficiency, detecting light with a peak-power wavelength of 8500 Å will exhibit a responsivity of approximately 0.68 amps/watt. Most commercially available PIN diodes exhibit a responsivity from 0.4 to 0.65 amps/watt. An optical communication system detector utilizing a PIN diode must include a small-signal amplifier because the incident optical power is relatively low, and hence the photo current in the bias circuit is very low. The noise-free voltage output,  $V(t)$ , of the entire detector system (Reference 11) can be expressed as:

$$V(t) = p(t)R * h(t)_{\text{diode}} * h(t)_{\text{amp-load}} \quad (39)$$

where \* denotes a convolution of impulse responses

$P(t)$  = incident optical power

$R$  = responsivity of the PIN diode

$h(t)_{\text{diode}}$  = impulse response of the photo diode (inverse  
Fourier Transform of detector frequency  
response)

$h(t)_{\text{amp-load}}$  = impulse response of load amplifier

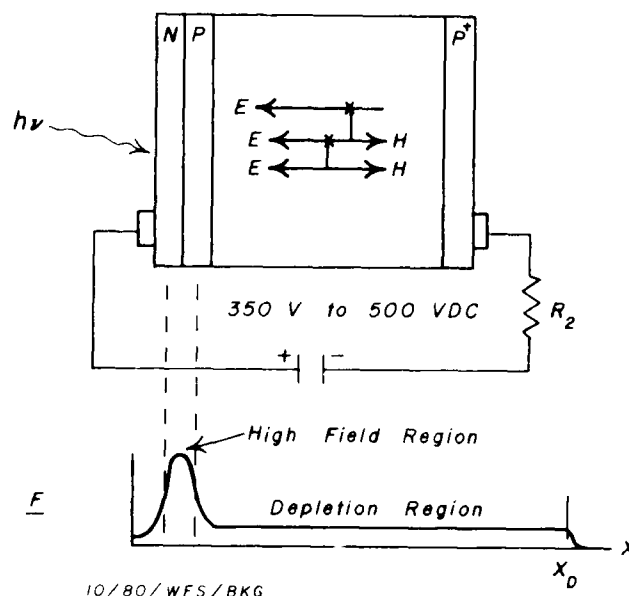
High quantum efficiency PIN diodes require a long absorption region. Conversely, a high frequency response necessitates very short drift times after the electron-hole pair has been created, and hence a short absorption region. Consequently, the manufacturer of PIN photodiodes must make a tradeoff between these two physical characteristics.

The PIN photodiode current is the sum of the displacement currents caused by generation of electron-hole pairs. As the precise instants of the generation of these electron-hole pairs are not predictable, an actual individual pulse shape usually differs from the average current pulse by an unpredictable amount. This variation in the shapes of the individual current pulses is known as signal-dependent noise (Reference 11), and has been discussed extensively in the open literature via mathematical noise models for PIN diodes.

## Avalanche Photodiodes

Receivers intended for optical waveguides operating over long distances often realize very low optical input levels, frequently on the order of a nanowatt. Consequently, the resulting photoelectron current of a few nanoamps is difficult to amplify to usable levels without the addition of a considerable amount of amplifier noise. It follows, therefore, that preamplification of the direct diode current prior to conventional electronic amplification, perhaps by an avalanche gain phenomenon, would be desirable. An "avalanche photodiode" exploiting this effect may be fabricated with a very heavily doped P region on one side of a depletion region, and a PN junction on the other side of the device (upper panel of Figure 89). A sharply defined very high field is manifested at this PN junction, as shown in the lower panel of Figure 89. As in the PIN photodiode described earlier, electron-hole pairs are generated in the depletion region of the device; however, an electron under the influence of the very high field gradient established in the vicinity of the PN junction can in turn produce tens or even hundreds of additional electron-hole pairs by collision ionization; the newly created secondary carrier pairs enhance the current created by the primary carriers by this avalanche effect, thereby amplifying the photodiode output current.

DIAGRAM AND ELECTRIC FIELD PLOT  
OF AVALANCHE PHOTODIODE



From *Fundamentals of Optical Fiber Communications*, ed. by M. K. Barnak, Academic Press, 1976, p. 160

Figure 89

Although the amplification factor should be a constant since the same number of electron-hole pairs generated by collision ionization should be realized from each photo-electrically generated primary electron, there is always a considerable variability in the number of secondary pairs created. This variability translates into an unpredictable current output for each photon absorbed in the depletion region. The statistical current fluctuation is in turn a "noise source" which very

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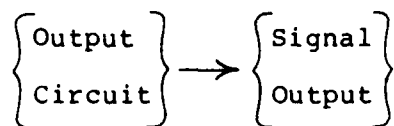
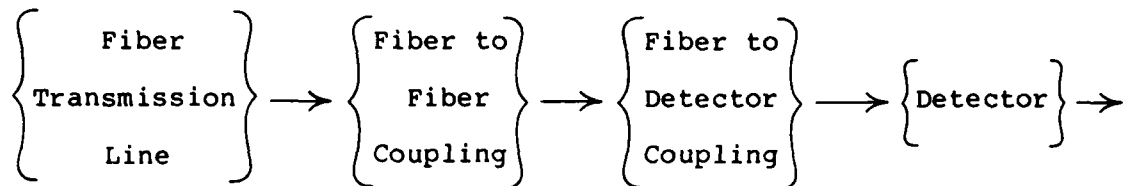
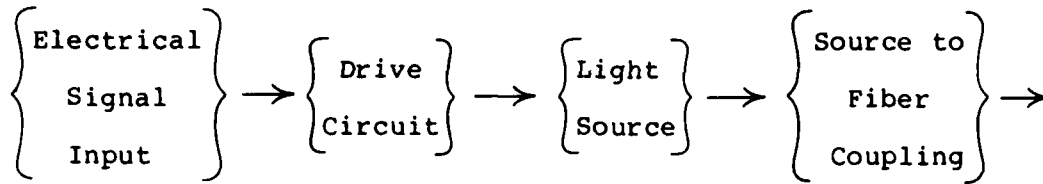
seriously limits the sensitivity of the device to a level well below that of an ideal electron multiplier. Collision ionization statistical noise is an additive effect to the signal noise discussed previously for PIN photodiodes (References 7,11). The designer of an avalanche photodiode tries to minimize avalanche noise by selecting very uniform materials so that the avalanche multiplication of electrons is not affected by statistical variations in the paths of the carriers traveling through the high field region. Secondly, the device is designed to force the creation of most of the primary electron-hole pairs outside of the high field region of the PN junction but within the depletion region, resulting in an avalanche photodiode with better multiplication statistics (References 7,11). Conversely, these primary electron-hole pairs must be created in the depletion region in as close proximity to the high field gradient region as possible to insure maximum frequency response. Although avalanche photodiodes fabricated with GaAsIn technology have demonstrated frequency responses up to 15 GHz in the laboratory, commercially available units of this design exhibit frequency responses in the range of 500 MHz to 10 GHz. These avalanche photodiodes exhibit good electron multiplication statistics, gains of a few hundred, and, if incorporating carefully designed antireflection coatings, realize quantum efficiencies approaching 100%.

Both PIN and avalanche photodiodes exhibit a background or "dark" current which is manifested even with no light photons incident on the device. The amplitude of this dark current is in the range of 10 picoamps to 10 nanoamps for both devices.

Unlike the PIN photodiode, the avalanche photodiode is extremely temperature sensitive. As the temperature varies, the bias voltage necessary to provide a constant avalanche gain (referred to as the responsivity of the device) varies considerably as well. The design of an avalanche photodetector must thus incorporate a highly controlled bias compensation to counteract the effects of the temperature sensitivity, a serious drawback of the avalanche photodiode. Nonetheless, in many cases the enhanced responsivity due to collision ionization electron-hole generation offsets the negative effects of the temperature sensitivity of the device. Since the avalanche multiplication process is very sensitive to bias, the user should be aware that nonlinearity of response and even saturation of the device can occur if the optical signal magnitude is very large (Reference 5).

#### Design and Analysis of an Optical Waveguide Communication System

A basic optical waveguide communications system using a current modulated light source consists of the following components:



Each of these optical components and their couplers will result in some loss of optical power as well as a degradation of system frequency response, both of which must be determined by the designer (an excellent discussion of the design and analysis of such a system is presented in an ITT technical note (Reference 22)). The designer of an optical communication system begins with the requirements of frequency response and length of the proposed optical waveguide communication system. Figures 90 and 91 show an example of a power throughput and risetime analysis of an hypothetical digital computer link. In this example, a 61 meter, 100 megabit/sec (RZ) optical communication system

Item

1)	Required bandwidth or bit rate:	100 Mb/s	
2)	Required distance:	61 M	
3)	Required SNR or BER:	$10^{-9}$	
4)	Fiber type:	Model T-301 ITT	PCS, 125 $\mu$ m core
5)	Total fiber bandwidth @ 10.5 MHz-km:		
6)	Source type: T-912 Laser	Average source coupled power, $P_s$ : -12 dB	$(-3)+(-6)+(-3)=-12$
7)	Detector type: PIN	Receiver sensitivity, $P_R$ : -29 dB	From manufacturer or chart for 100 Mb/s, RZ system
8)		Total Margin, $(P_R - P_s)$ : 17 dB	
9)		Total fiber loss @ 35 dB/km: 2.2 dB	35 db x 61/1000 = 2.135 db
10)	No. connectors: 2	Total connector loss @ 1 dB/conn: 2 dB	
11)	No. splices: 0	Total splice loss @ 0.3 dB/splice: 0 dB	
12)		Detector coupler loss: 1 dB	
13)		Allowance for temperature degradation: 3 dB	
14)		Allowance for time degradation: 3 dB	
15)		Total waveguide attenuation: 11.2 dB	
16)		Excess power [(total margin)-(total waveguide attenuation)]: 5.8 dB	

Revised From: ITT Optical Fiber Communication Technical Note R-1

Figure 90

POWER THROUGHPUT ANALYSIS WORKSHEET

Item

1) Required system risetime:	$3.5 \times 10^{-9}$ sec (100 Mb/sec RZ)			
2) Required fiber length, type:	61 Meters, Pcs T-301	<u>RISETIME</u>	<u>RISETIME</u> <u>SQUARED</u>	<u>COMMENTS</u>
3) Source type:	T-912 Laser	1.5 nsec	2.25	Manufacturers data
4) Total fiber risetime due to multi mode dispersion @ 33 nsec/km:		2.013 nsec	4.052	$33 \times 10^{-9} \times \frac{61}{1000} = 2.013$ nsec
5) Total fiber risetime due to material dispersion @ 0 nsec/km: (Typically 5.5 nsec/km for LEDs, negligible for lasers)		0 nsec	0	due to laser light
6) Detector type:	PIN	1 nsec	1	Manufacturers data
7) Receiver (if analog):		- nsec	-	
8)	SUM OF SQUARES:		7.302	
9) System risetime, (1.1) (Square root of sum):	<u>2.97 nsec</u>			

Analog system - 3 dB electrical bandwidth,  $(.35 \div \text{system risetime})$ :

Revised from: ITT Optical Fiber Communication Technical Note R-1

Figure 91

RISETIME ANALYSIS WORKSHEET

bit error rate (BER) of one part in a billion ( $10^{-9}$ ) is to be designed and fabricated. From a list of manufacturer-supplied fiber, source, and detector physical characteristics, a fiber

is selected which will meet or exceed the specified bit rate and optical transmission characteristics. For this example a PCS 125  $\mu\text{m}$  core (ITT Model T-301) was chosen. Although this fiber exhibits an attenuation of 35 dB/km, a loss of only about 2.2 dB ( $35 \text{ dB} \times \frac{61}{1000} \approx 2.2 \text{ dB}$ ) is realized for the 61 meter system (Figure 90, Item #9). The risetime of the selected fiber is 33 nsec/km (due to multimodal dispersion), and the fiber exhibits a multimodal dispersion of 2.013 nsec ( $33 \text{ nsec} \times \frac{61}{1000} = 2.013$ ) for the example 61 meter system. Since a laser has been selected as a light source in this example, the resulting nearly monochromatic light therefrom will experience a negligible amount of material dispersion (Figure 91, Items 4 and 5).

The variation of output power between otherwise identical sources must be accounted for in the analysis. A light source with an output power of 1 milliwatt (mW) is considered a standard, and is said to have 0 dB loss; sources exhibiting an output optical power greater than 1 mW are given a + dB rating, while those exhibiting less than 1 mW output power are given a negative dB rating. An ITT, T-912 laser with graded index pigtail was chosen for the light source for this example. The manufacturer rates its output power at 0.5 mW, i.e., 3 dB less than 1 mW; its peak output power is therefore rated as -3 dB. Since the data format to be used is RZ, the average light source output is 6 dB less (assuming a 50% distribution of logic HIGHS in the data stream). To extend the life of the laser the drive

current will be halved from that recommended by the manufacturer resulting in an added 3 dB loss, for giving a total value of -12 dB for the power source (Figure 90, Item 6). The rise time of 1.5 nsec for this laser is considerably less than the 3.5 nsec risetime required for the specified 100 megabits/sec system (Figure 91, Item 3). From manufacturer's data it is determined that the PIN photodiode chosen for the system detector will be adequately sensitive at -29 dB optical power at the 100 megabit/sec RZ data rate (Figure 90, Item 7), and that the PIN photodiode will exhibit a risetime of 1 nsec (Figure 91, Item 6).

As shown in Figure 90, Item 10 through 14, connector loss factors (Item 10) may be obtained from a manufacturer-supplied data table. Fiber splices will not be required in this short 61 meter system. The detector coupler loss is 1 dB (Item 12); a conservative estimate of loss resulting from thermal and aging degradation of 3 dB for each connector is used in this example (Figure 90, Items 13 and 14). Thus, the total attenuation of the fiber optic system is computed to be 11.2 dB (Figure 90, Item 15). The difference between the average source-coupled power (Figure 90, Item 6) and the receiver sensitivity (Figure 90, Item 7), calculated as 17 dB, represents the total margin which must not be exceeded by losses in the fiber link and its coupling. Figure 90, Item 15, shows that the proposed fiber link will exhibit a total attenuation of 11.2 dB, resulting in an excess power of 5.8 dB. Thus, the operational system will

exceed the initial optical power specification for a 61 meter optical transmission link operating at a data rate of 100 megabits/sec. Finally, the optical waveguide communication system risetime may be calculated (Figure 91, Item 9) by computing the square root of the sum of the squares of the risetimes of each component, and multiplying the result by 1.1. The calculated risetime of 2.97 nsec is well within the specified 3.5 nsec risetime (100 megabits/sec) of the proposed system.

Although usually not a limitation of such a system design, an approximately 4% reflection of light at the ends of the fiber is a typical phenomenon which slightly degrades overall performance. Other forms of energy loss in a long optical fiber are of such magnitude that the effects of these reflections are negligible. However, for a system exhibiting a very high fiber transmission factor and of a very short length, reflection effects may be realized as a form of system noise. For very long fiber communications channels, the optical transmission system would almost certainly require splices, fiber-to-fiber couplings, and repeaters. A repeater consisting of a PIN or ADP photodiode, an amplifier, wave shaping circuit, and a transmitter, is generally inserted into the line every ten or twenty kilometers to strengthen and reshape the optical signal.



## Integrated Optics

Variations in the magnitude of an electric field through a crystal such as Lithium Niobate are capable of modulating the interatomic spacing of the material, creating variations in its index of refraction by slight alterations in the local density of the electron charge cloud. This modulation of the index of refraction in turn creates a phase shift in polarized monochromatic light transmitted through the material. If a beam of polarized laser light is shifted in phase by  $180^\circ$  in this manner, and then is summed with a second beam of polarized monochromatic light from the same source which has experienced no phase shift, the two beams cancel one another and no output light will be detected. Conversely, the two beams add in intensity if no electric field is applied to the crystal, and thus no phase shift is experienced by the light beam propagating through the optical channel which includes the crystal. These physical principles have been exploited in the fabrication of integrated optical devices such as electro-optical switches, logic elements, beam deflectors, A/D and D/A converters. Dual beam lasers and convolvers have also been fabricated in the laboratory, while integrated LED and/or laser arrays may be purchased from commercial companies such as Laser Diode, Inc. Bell Laboratories of Holmdel, NJ, has recently reported fabrication of Lithium Niobate ( $\text{LiNbO}_3$ ) crystal switches which may be used with either TM or TE polarized light.

## Recent Developments and Future of Optical Waveguides

In an effort to exploit the very low attenuation of glass fiber optic waveguides for high data rate transmission over distances of many kilometers, there have been several reports of successful fabrication of solid-state injection CW lasers operating in the 1.1-1.55  $\mu\text{m}$  region of the optical spectrum. Nippon Telegraph and Telephone Corporation reported that their Masashino Electrical Communication Laboratory fabricated single IDL (InGaAsP) devices with peak emitted power at 1.29  $\mu\text{m}$ . These devices have been tested on several fiber optic systems of different lengths with the following performance data: 1) a 30 km system operating at 100 megabits/ $\mu\text{sec}$ ; 2) a 23 km system operating at 1.2 gigabits/sec; and 3) a 15 km system operating at 1.6 gigabits/sec. These investigators reported that they expect even better results at a transmission wavelength of 1.5  $\mu\text{m}$ , providing the fiber optics core cladding index difference is shifted from 0.2% for the 1.29  $\mu\text{m}$  system to 0.6% for the 1.5  $\mu\text{m}$  system to minimize dispersion (Reference 14). California Institute of Technology has also reported the integration and interconnection of transmitters, repeaters and detectors which operate above 1 GHz (Reference 14). Hitachi, Ltd. of Tokyo, Japan, has reported the development of laser and FET devices integrated on the same chip which exhibit risetimes of .4 nsec (Reference 8). Bell Laboratories of Murray Hill, NJ, have recently reported 5  $\mu\text{m}$  stripe heterostructure ILD's fabricated

with InGaAsP which exhibit outputs of 500 mW without catastrophic damage to the mirror at each end of the device (mirror damage is typically realized at about one-half that level in GaAlAs devices (Reference 14)). Bell Laboratories has indicated that by 1990 transatlantic fiber optic communication systems utilizing ILD lasers ( $\lambda = 1.3-1.55 \mu\text{m}$ ) will operate at 274 Mb/sec, with repeaters every 30 to 50 kilometers (Reference 14).

Detectors with an "on chip" preamp are available from Spectronics, Inc. of Richardson, TX, at a low cost, albeit with a relatively low data rate capacity of 1 megabit/sec. The fastest commercial photodiode known to the author of Part III of this report (W.F.S.) is the Model 403B of Spectra-Physics of Mountain View, CA, which exhibits a risetime of less than 50 psec in response to a 5 psec pulse from a 600 nm synchronously pumped dye laser. Exxon Enterprises, Inc. manufactures complete transmitter and receiver plugin modules with TTL or ECL compatability. The OTX5100 laser ECL compatible transmitter is usable to 275 megabits/sec NRZ, featuring output stabilization via current feedback, and onboard voltage regulation and transient protection. The PIN receivers respond to 150 megabit/sec NRZ pulses at present, to be followed soon by a receiver in the frequency range of 275 megabits/sec NRZ which will be compatible with the OTX5100 transmitter. Sumitoma Electric of Higashi-ku, Osaka, Japan, produces a host of analog and digital optical communication systems, including multidrop systems in

which a beam splitter is used to merge with or depart from a main transmission line, as well as an optical directional filter to facilitate either two-channel multiplex transmission or the simultaneous two-way transmission of signals in the same fiber.

Simultaneous transmission of many signals in a single fiber is also possible by the utilization of a Bragg cell actually fabricated as an integral part of a fiber. By etching an optical grating in the fiber cladding, in which the distance,  $d$ , between each grating is related to an integral number of light wavelengths, it is possible to couple light of wavelength  $\lambda$  into the fiber light. If allowed to impinge on the fiber at an angle of  $90^\circ$  to the "plane" of the grating, the light coupled into the fiber in this manner (Reference 7) is deflected or "trapped" into the waveguide through an angle called the Bragg angle ( $\phi$ ):

$$d \sin \phi = \frac{2\pi m}{\lambda} \quad (40)$$

where:  $d$  = distance between etched gratings

$\lambda$  = wavelength of laser light

$m$  = order of interference, i.e., the number of wavelengths between each grating.

If several groups of these gratings are etched on both ends of the fiber in such a manner that each group is receptive to

light of a different wavelength, many wavelengths may be coupled into and out of the same fiber. Consequently it is possible to realize simultaneously many communication systems, each operating at a different wavelength, in the same fiber with no crosstalk between the systems.

Fiber optics have been used to replace the wiring harness of aircraft and it is contemplated that a growing number of airplanes and automobiles will use glass fiber ("wiring") harnesses in the next two years. Beginning in 1983, General Motors plans a 400 Hz fiber system for the control systems of some of its passenger cars to cut costs and weight, and to circumvent problems of electromagnetic interference (Reference 23). New federal regulations are now motivating the development of fiber optics in passenger cars to solve these interference problems.

Data transmission capabilities of optical fibers will increase in the next ten to twenty years. A new fiber optics fiber fabricated from thallium bromoiodide, referred to as KRS-5 and specifically designed for the 10 micron output of a CO<sub>2</sub> laser, has been reported in a recent publication from Hughes Research Laboratories. Among other advantages, this system exhibits extremely low losses of .001 dB/km and may prove to be useful for future long distance optical communications systems (Reference 25). It is estimated that by the Year 2000, graded-index fiber maximum data transfer rates will be

approximately 10 gigabits/km, with systems operating in the infrared region (1.1 to 1.5  $\mu\text{m}$ ). Single mode fibers will be used for long distance, high data rate transmission (nearing 75-80 gigabits/km by the Year 2000) thereby greatly reducing the number of repeaters necessary. Solid-state light emitters will exhibit output power of several watts for lasers and several tenths of a watt for a low cost hemispheric L.E.D., with life expectancies of these devices of 100,000 hours or greater. Miniature, precision demountable connectors will be available at low cost due to high volume production.

A list of fiber optic terms and definitions is presented below, as is a list of manufacturers of fiber optic transmission systems and components.

#### Fiber Optics Terms and Definitions

Absorption Losses - Losses caused by impurities, principally by water, transition metals and other elements (Cr, Mn, Fe, Co, Ni), and by intrinsic material absorption.

Acceptance Angle - Any angle measured from the longitudinal axis of the fiber to the maximum angle at which an incident ray will be allowed to enter the waveguide. The maximum acceptance angle is governed by the indices of refraction of the two media.

Acceptance Cone - A cone defined by an angle equal to twice the acceptance angle.

Axial Ray - A ray passing through the axis of the optical waveguide without any internal reflection.

Cladding - A sheathing or covering, usually of glass or plastic, fused to the core of high-index material.

Coherent Bundle - A group of optical fibers assembled such that the relative positions of the ends of any fiber within the bundle are simply related and are maintained throughout the length of the fiber. This relationship allows each fiber to act as an independent channel, in turn permitting information concerning the spatial distribution of intensity of the light beam to be transferred through such bundles (e.g., an image formed on the input face will be transmitted intact to the output face).

Core - The center dielectric in an optical fiber whose index of refraction is greater than that of its surrounding medium, usually a cladding.

Core Packing Fraction - The fractional area occupied by core material in a group of optical fibers assembled together to form an area. For hexagonally-packed fibers, the fractional area occupied by cores is given by:

$$F_C = \frac{\pi}{2\sqrt{3}} \frac{d^2}{D^2} \approx 0.91 \frac{d^2}{D^2} \quad (41)$$

where D = overall fiber diameter

d = core diameter

Coupling Lens - A device used to couple optical power efficiently between low numerical aperture optical fibers.

Coupling Loss (expressed in dB) - The amount of power in the fiber optic link lost at discrete junctions, including source-to-fiber, fiber-to-fiber, and fiber-to-detector boundaries.

Critical Angle - The angle subtended by the reflected ray in an optical waveguide when the ray enters the core at the maximum half-angle of the acceptance cone (the maximum acceptance angle).

Dark Current - The output current that a photodiode emits in the absence of incident light.

Data Bus Coupler - An optical component used to interconnect a number of terminals through optical waveguides, thereby providing an inherently bi-directional system by mixing and splitting all signals in the component. Sometimes referred to as a star coupler.



**Fiber Bundle** - A group of parallel optical fibers over which a loose-fitting polyvinyl-chloride (PVC) jacket has been extruded. The number of fibers in such a bundle may range from a few to several hundreds depending on the application and the characteristics of the fiber.

**Fiber Optic Cable** - A sub-assembly made up of several optical fibers incorporated into an assembly of organic materials which provide the necessary tensile strength, external protection, and handling properties comparable to those of equivalent diameter coaxial cables.

**Fiber Optics** - The technique of conveying light or images through a particular configuration of glass or plastic fibers. Fiber optics can be categorized roughly into three groups: incoherent, coherent, and specialty: 1) incoherent fiber optics will transmit light, but not an image; 2) coherent fiber optics will transmit an image through perfectly aligned, small (10-12 micron), clad, optic fibers; and 3) specialty fiber optics combine several aspects of 1 and 2.

**Fresnel Reflection** - Reflection losses incurred at the input and output faces of the fiber, resulting from differences in refractive index between the core glass and the immersion medium. For normal incidence, this can be expressed by:

$$A_F = \frac{(n_2 - n_1)^2}{(n_2 + n_1)^2} \quad (42)$$

where  $A_F$  = Fraction of incident light reflected

$n_2$  = Index of refraction of core

$n_1$  = Index of refraction of immersion medium. (For  
air  $n_0 = 1.00$ )

**Graded Index Fiber** - An optical fiber which has a refractive index which becomes progressively lower with increasing distance from the fiber longitudinal axis. This characteristic causes the light rays to be continually refocused by refraction in the core.

**Index Matching Fluid** - Used to minimize fresnel losses by making minute particles optically transparent and reducing refractive index differences.

**Index of Refraction (relative)** - The ratio of the velocity of light in one medium to the velocity of light in another medium.

**Index of Refraction (absolute)** - The ratio of the velocity of light in a given medium to the velocity of light in a vacuum. Because the density of air is so small, it is convenient to consider the velocity of light in air the same as its velocity in a vacuum.

$$n_0 = \text{Index of Refraction of Air} = \frac{V_{\text{Vacuum}}}{V_{\text{air}}} = \frac{186,000 \text{ mi/sec}}{186,000 \text{ mi/sec}} = 1.00$$

$$n_{\text{Water}} = \frac{V_{\text{Vacuum}}}{V_{\text{Water}}} = \frac{186,000 \text{ mi/sec}}{139,500 \text{ mi/sec}} = 1.33$$

Infrared - Those wavelengths longer than 770 nanometers.

Infrared is used extensively in the transmission of light through optical waveguides.

Lambertian Source - A source that appears equally bright from all directions. Lambertian sources emit a flux proportional to the cosine of the angle from the normal.

LED (Light-Emitting Diode) - A PN junction device which emits light radiation when biased in the forward direction.

Light Conduit (Light Guide) - A flexible, incoherent bundle of fibers used to transmit light.

Light Detector - An output device, such as a PIN photodiode, which converts detected light into an electrical signal.

Light Guide - A large number of optical fibers assembled as a composite component which is used solely to transmit light flux.

Light Leakage Losses - Losses due to imperfections at the core/cladding boundary of a graded or step index fiber.

Meridional Ray - A ray that passes through the axis of a fiber while being internally reflected (in contrast with a skew ray), and which is confined to a single plane.

Multifiber - A coherent bundle of fused single fibers that behaves mechanically as a single glass fiber.

Multi-Mode - An optical waveguide with a relatively much larger core (1 to 3 mils) than the single-mode waveguide core (2 to 8 microns), which permits the propagation of approximately 1000 optical modes.

Non-Coherent Bundle - A group of optical fibers positioned essentially parallel to each other in a bundle, used as a means of guiding beams of light. A Light Guide.

Numerical Aperture - The numerical aperture (NA) of an optical fiber defines a characteristic of the fiber in terms of its acceptance of impinging light. The "degree of openness," "light gathering ability" and "acceptance cone" are all terms describing this characteristic. The light accepted by a fiber, in air, has a definitive relationship to the combined core/cladding construction of the fiber, as may be observed from the formula for meridional rays.

$$NA = \sqrt{n_2^2 - n_1^2}$$

where  $n_2$  = index of refraction of the core

$n_1$  = index of refraction of the cladding

**Optical Break** - The breaking of an optical fiber in a way which produces flat end surfaces perpendicular to the longitudinal axis of the fiber.

**Optical Waveguide** - A guidance system cylindrical in shape, of transparent dielectric material of refractive index  $n_1$ , whose walls are in contact with a second dielectric material of a lower refractive index  $n_2$ ; alternately, a dielectric material core which exhibits a refractive index that becomes progressively lower with increasing distance from the longitudinal axis.

**Pulse Dispersion** - (Pulse Spreading) - The separation or spreading of the input characteristics of a pulsed optical signal which occurs as the pulse traverses the length of the optical fiber, thereby limiting the useful transmission bandwidth of the fiber. Dispersion is expressed in units of nsec/km. Three mechanisms of dispersion are the material effect, the waveguide effect, and the multimode effect.

**Radiance** - The radiant flux per unit solid angle and per unit surface area measured normal to the direction of propagation of the flux.

Radiation Pattern - The output radiation intensity as a function of output angle.

Receiver Sensitivity (expressed in dBm) - A measure of the optical power which the photodetector must receive to achieve a specified baseband transmission performance, such as a specified bit-error rate or signal-to-noise ratio.

Reflectance Losses - (See Fresnel Reflection)

Scattering Losses - Losses caused by microheterogeneities, including undissolved particles, boundary roughness and intrinsic scattering.

Single Fiber - A filament of optical material, glass or plastic, usually drawn with a lower-index cladding. (See Optical Fiber)

Single-Mode - One type of low-loss optical waveguide with a very small core (2-8 microns), requiring a laser source because of the very small entrance aperture of the waveguide. The small size of the core radius is approximately the same as the wavelength of the source; consequently, only a single mode is propagated.

Skew Ray - A ray, sometimes referred to as a dominant ray, that never intersects the axis of a fiber while being internally reflected (in contrast with a meridional ray).

Source Optical Power (expressed in milliwatts) - The total amount of optical power emitted by the light source used.

Spectral Width (expressed in angstroms) - This depicts the wavelengths of the light emitted by the source.

Step-Index Fiber - An optical fiber exhibiting an abrupt change in refractive index at the physical boundary of a core and cladding possessing different indices of refraction.

Tee Coupler - An optical component used to interconnect a number of terminals through optical waveguides, utilizing partial reflections at dielectric interfaces or metallic surfaces, or a bifurcation of the optical waveguide bundle.

PAPERS PUBLISHED OR IN PRESS SUPPORTED BY THIS U.S. AIR FORCE  
RESEARCH CONTRACT

Papers Published

1. Gilbert, B. K., L. M. Krueger, and R. D. Beistad: Design of prototype digital processors employing subnanosecond emitter coupled logic and rapid fabrication techniques. IEEE Transactions on Components, Hybrids, and Manufacturing Technology CHMT-3(1):125-134 (March) 1980.
2. Gilbert, B. K. and L. D. Harris: Advances in processor architecture, display, and device technology for biomedical data processing. IEEE Transactions on Nuclear Science NS-27(3):1197-1206 (June) 1980.

Papers In Press

1. Gilbert, B. K., L. M. Krueger, and T. M. Kinter: Advances in the processing of large biomedical data bases using specialized computers, improved device technology, and computer-aided design. To Appear in the Proceedings of the 1980 Joint U.S.-France Conference on Biomedical Image Processing, Grenoble, France, May 27-31, 1980, Springer-Verlag Press (In Press).



2. Gilbert, B. K., R. D. Beistad, and L. M. Krueger: A hierarchical network of general-purpose and special-purpose MIMD processors for the computation of large computed tomography data bases. Proceedings of Second International Conference on Distributed Computing Systems, Paris, France, April 8-10, 1981 (Submitted).
3. Gilbert, B. K., S. K. Kenue, R. A. Robb, A. Chu, A. H. Lent, and E. E. Swartzlander, Jr.: Rapid execution of fan beam image reconstruction algorithms using efficient computational techniques and special purpose processors. IEEE Transactions on Biomedical Engineering Vol. BME-28(2) (February) 1981.
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List of Special Parts Used In or Developed For this Research Project

<u>Description</u>	<u>Manufacturer</u>	<u>Part Number</u>
100 ohm terminations	Epitek Electronics, Ltd.	L1206-101G
470 ohm terminations	Epitek Electronics, Ltd.	L1211-471G
85 ohm terminations/bypass capacitor	Epitek Electronics, Ltd.	3B14000
SMA coax adaptor	Augat, Inc.	101-HG1
50 ohm wire-wrappable coax cable	W. L. Gore and Associates, Inc.	CXN1213
75 ohm wire-wrappable coax cable	W. L. Gore and Associates, Inc.	CXN1233
70 ohm semi-rigid coax	Uniform Tube, Inc.	UT47-70
75 ohm multi coax cable	Amp Special Industries	1-226-807-0
93 ohm multi coax cable	Amp Special Industries	1-226-812-0
Scotchflex 13 pair ribbon cable	3M, Electronic Products Division	3365-26
Scotchflex 20 pair ribbon cable	3M, Electronic Products Division	3365-40
13 pair woven twisted cable	Woven Electronics, Inc.	T-13TP2807UL1568N
20 pair woven twisted cable	Woven Electronics, Inc.	T-20TP2807UL1568N
24-contact leadless chip carrier	3M, Electronics Products Division	ST-88-524-AC
3.3 $\mu$ f, 10 VDC tantalum electrolytic capacitors	Fujitsu America, Inc.	CS90E-1A-3R300-R58
.01 $\mu$ f, 100 VDC X7R ceramic capacitors	AVX Ceramics Corporation	DG011C103M
.1 $\mu$ f, 50 VDC X7R ceramic capacitors	AVX Ceramics Corporation	DG015C104M
Subnanosecond ECL dual in-line package logic panel	Augat, Inc.	X8136-ECL 117-2

Some Manufacturers of Optical Communication Systems or Components

Manufacturer	Address	Phone #	Products
1) Amp Inc.	Harrisburg, PA 17105	(717)564-0100	C*
2) B & H Electronics Co.	Box 490, Chester, NY 10918	(914)782-0366	LS(T),D(R)
3) Corning Glass Works	Telecommunications Product Department Houghton Park Corning, NY 14830	(607)974-8812	F
4) Deutsch	Optical Waveguide System Municipal Airport Banning, CA 92220	(714)849-7822	C
5) El duPont de Nemours and Co.	1007 Market Street Wilmington, DE 19898	(302)774-2421	F
6) Edmund Scientific Co.	101 East Gloucester Pike Barrington, NJ 08007	(609)547-3488	F,CA
7) EG and G Inc.	Electro-Optics Division 35 Congress Street Salem, MA 01970	(617)745-3200	D
8) Eudae Co.	OPS Division PO Box 577 Los Angeles, CA 90066	(213)828-0694	S
9) Galileo Electra Optics Corp	Galileo Park Sturbridge, MA 01518	(617)347-9191	T,D
10) General Electric Co.	Semiconductor Products Division West Genessee Street Auburn, NY 13021	(315)253-7321	T,D
11) General Fiber Optics Inc.	Box 82 Caldwell, NJ 07006	(201)228-4400	F,T,D,CA
12) General Optics Corp.	3005 Hadley Road South Plainfield, NJ 07080	(201)753-6700	LS,T

**\*KEY**

SP = Splicers

LS = Light Sources  
(L.E.D. and/or laser)

CA = Fiber Optic Cables

T = Transmitters

R = Receivers

C = Connectors

F = Fibers

D = Detectors

S = Optical Communication Systems

13) Hewlett Packard Co.	640 Page Mill Road Palo Alto, CA 94304	(415) 557-1501	LS,D,T,R,F,S,
14) Hitachi American Ltd.	Electronics Division Sales and Services Division 707 West Algoquin Road Arlington Heights, IL 60005	(312) 593-7660	T,LS
15) Hughes Aircraft Co.	5250 West Century Blvd. PO Box 90515 Los Angeles, CA 90009 Dr. Ron Burns Project Engineer - Fiber Optics	(714) 670-1515 X5964 (714) 752-3857	S,F Military Only
16) ITT	Electro Optical Products Division 7635 Plantation Road Roanoke, VA 24019	(703) 563-0371	F,T,D,R
17) Laser Diode Labs Inc.	1130 Somerset Street New Brunswick, NJ 08901	(201) 249-7000	LS,T
18) LeCroy Research Systems Corp	The Fiberoptic Division 10024 York Road Cockeysville, MD 21030	(301) 628-2240	T,R,S,
19) Math Associates Inc.	376 Great Neck Road Great Neck, NY 11021	(516) 466-9818	T,R,S,CA
20) Meret Inc.	1815 24th Street Division Santa Monica, CA 90404	(213) 828-7496	T,R,S
21) Minnesota Mining and Manufacturing Co.	Electronics Product 3M Center St. Paul, MN 55101	(612) 733-1110	S
22) Motorola Semiconductor Products Inc.	PO Box 20912 Phoenix, AZ 85036	(602) 244-6900	LS,T,R,D
23) Optical Information System Exxon Enterprises Inc.	350 Executive Blvd. Elmsford, NY 10523	(914) 345-5850	T,R,S
24) Orionics Inc.	1238 Ortiz SE Albuquerque, NM 87108	(505) 268-8388	SP



25) Photodyne Inc.	5356 Sterling Center Drive West Lake Village, CA 91361	(213)889-8770	Absolute Measurement Devices for Fiber Optic Communication System Phys- ical Charac- teristics
26) Plessey Opto- electronics and Microwave	1641 Kaiser Avenue Irvine, CA 92714	(714)540-9934	T,R
27) Poly-Optical Products Inc.	1815 East Carnegie Avenue Santa Anna, CA 92705	(714)957-9288	F
28) Quartz Products Corp.	Box 1347 Plainfield, NJ 07061	(201)757-4545	F
29) Raytheon Data Systems	Telecommunication Division Norwood, MA 02062	(617)762-6700 X341	T,R
30) RCA Electro Optics and Devices	RCA Solid State Division New Holland Avenue Lancaster, PA 17604	(717)397-7661	LS,T,D,R,S,
31) Siedor Optical Cables Inc.	631 Miracle Mile Horseheads, NY 14845	(607)739-3562	LS,D
32) Spectronics Inc. (a division of Minneapolis Honeywell Inc.)	830 East Arapaho Road Richardson, TX 75080	(214)234-4271	T,R,F,S
33) Sumetoma Electric Indus- tries, Inc.	5627 Haward Street Niles, IL 60648	(312)647-8293	LS,T,D,R,F,S
34) Valteo Corp.	99 Hartwell Street West Boylston, MA 01583	(617)835-6082	T,R,F,CA,S

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